ANNEXURE - IV

ANNEXURE IV (A) - PRE-QUALIFICATION CRITERIA

The evidence of Photonics Chip Fabrication Foundry Facility in India along with following details must be submitted:
a) Infrastructure and Technical Capabilities
b) Address of 3 users during last two years

ANNEXURE IV (B) – TECHNICAL SPECIFICATIONS

	TECHNICAL SPECIFICATION OF SILICON PHOTONIC CHIP TAPE OUT IN SILICON ON INSULATOR PLATFORM	
A.	**SILICON ON INSULATOR SPECIFICATIONS**	
1	Silicon Substrate Thickness	~ 700 µm
2	Buried Oxide (BOX) Thickness	~ 2 µm
3	Silicon Device Layer Thickness	220 nm
4	Top Cladding Material	Silicon Dioxide
5	Top Cladding Thickness	~ 3 µm
6	Doping Type of Silicon Device Layer	P type
7	Doping Concentration of Silicon Device Layer	1e15 cm^{-3}
B.	**DESIGN FLEXIBILITY**	
1	Waveguide Etch Depths	220 nm, 130 nm, 70 nm
2	Min Waveguide Width	130 nm
3	Min Separation Between Two Waveguides	200 nm
4	Waveguide Width Variation	± 25 nm
5	Etch Depth Variation	± 10 nm
6	Waveguide Loss	< 3 dB/cm
7	Tapering Between Different etched Waveguides	Must Have
C.	**DEVICE LIBRARY REQUIREMENTS: PASSIVE**	
1	Grating Coupler	
	a. Inclined Angle with Vertical	10 degree
	b. Peak Wavelength	1550 nm
	c. Coupling Loss	< 6 dB/facet
	d. 1 dB Bandwidth	20 nm
2	Edge Coupler: Coupling Loss	< 3 dB/facet
3	Power Splitter(2 × 2 and 1 × 2)	
	a. Splitting Efficiency at 1550 nm	3 dB
	b. Insertion Loss	< 0.2 dB
4	Waveguide Crossing	
	a. Insertion Loss	< 0.2 dB
	b. Crosstalk	< - 40 dB
5	Polarization Beam Splitter (1 × 2)	
	a. Insertion Loss	< 0.3 dB

D.	BACK END SPECIFICATIONS	
1	Number of Metal Layers	≥ 2
2	Sheet Resistance of Metal Layers	25-45 milli ohm/square
3	Metal Heater for Waveguide Tuning	
	a. Material	TiN
	b. Sheet Resistance	10-14 ohm/square
	c. Distance From Top of The Waveguide	~ 2 µm
	d. Minimum Width	2 µm
4	Top Cladding Bond Pad Opening	$> 50\times50$ μm^2
5	Options for Top Cladding Oxide Opening upto BOX	YES
6	Deep Trench For Edge Coupling	YES
E.	DEVICE LIBRARY REQUIREMENTS: ACTIVE	
1	Required Doping concentration (Both p and n type)	1e18 cm^{-3} ,2.5e19 cm^{-3}
2.	Modulator	
	a. Insertion Loss	< 4 dB
	b. Vπ	< 10 Volt
	c. VπL	< 2.5 Volt-cm
	d. Bandwidth	> 35 GHz
3	Photo Detector	
	a. Responsivity	> 0.85 Amp/Watt
	b. Bandwidth	> 35 GHz
	c. Dark Current	< 50 nano Amp
F.	REQUIRED DOCUMENTATIONS	
1	Device Library Book	Photonic Design Kit should be compatible with Ansys Lumerical
2	Layout and Technology Handbook	GDS II sample LayOut file should be provided
3	Design Rule Check Script	Should be compatible with KLayout
G	CHIP DIMENSION: 3×16 mm^2	
H	NUMBER OF DIES: At least 15	
I.	DELIVERY TIME:	
J.	Parent company should be an established company with good number of silicon photonic Multi Project Wafer runs (at least 50, Wafer size – 200/300 mm)	
K		
L.	OPTIONAL	
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NOTE: The bidder has to provide a Technical compliance statement - Mentioning (Complied / Not complied)