Technical specification for proposed
Circuit and system simulation suite

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<tr><th>Sr. No.</th><th>Specification</th></tr>
<tr><td>1.</td><td>Circuit and system simulation suite
Should be a comprehensive unified software solution covering design, simulation, layout, extraction and verification of analog circuits, digital circuits, printed circuit boards, and electromagnetic structures with the following general features and specific features listed in later items

Should have the capabilities of running Analog, Digital, Mixed Language and Mixed Signal simulation
Should support RF IC Design, 3D IC Design.
Should support submicron and deep submicron technologies
Should provide the libraries for 180nm, 90nm, 45nm, 28nm & 16nm as part of the package
Should support the multimode simulation settings providing different simulation engines for fast transistor simulation, threading for fast simulation analysis.
Should have the feature of providing constraints for Layout at the schematic level
Should support different Analog Layout Techniques like Common Centroid, Interdigitation, constraint driven placement and routing.
Should support the feature of configuring physical hierarchy
Should support the design rule driven layouts
Should support the analysis of results and support post processing
Physical synthesis tool should support timing analysis, report generation, netlist generation of different formats, constraint generation for downstream tools
Static Timing Analysis (STA) sign-off tool
Should support scan logic insertion, Memory BIST generation, building fault models, verifying test structures, debug design rule violations, ATPG Pattern generation.
Should support Logic Equivalence Check at different stages of the design cycle
Should support Low power implementation
Should support Low power verification
Should support Custom Analog, Digital ASIC and Mixed Signal Designs
Should provide the capability to route complete chip using chip assembly or space based routers providing the access to scripting like tck / perl
Physical implementation tool should support the features for Floorplanning (Manual, Automatic), Powerplanning, Placement of standard cells (automatic, manual), Clock Buffer Insertion, Timing Violation fixing, ECO, Power Routing, Chip Level Routing etc.
Power analysis tool
SI analysis (covers crosstalk, delay, noise analysis) tool
IR drop & EM analysis tool
Should support Design Rules Checking(DRC), Electrical Rule Checking (ERC), Layout vs Schematic (LVS), (common for Digital & Analog/ Mixed Signal flow)
Should support extraction of parasitic elements like R, C, L, M (common for Digital & Analog/ Mixed Signal flow)
Should provide the feature of generating different standard parasitic netlists like, DSP, SPEF, HSPICE, SPICE, SPECTRE,
Should support characterization of libraries for power, noise and timing
Should support the feature to generate liberty files from custom designs
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2.	**Design exploration platform:** **The design exploration platform should have the following features:** • Work seamlessly with the design environment for single test operation; Design exploration with sweeps, corners, and Monte Carlo analysis across multiple test benches and conditions; Support of matching and correlation constraints from the schematic editor; Creation and tracking of parametric dependencies among tests for more complex analysis; Integrates with Simulation Platform; Ability to save different test configurations for different steps in the testing flow and analysis of results; Creation of specifications directly from simulation results; Quick overview window of test results against target specification; Cross-probing and annotation to schematics and layout; Support for pre-run calibration scripting Built-in variation analyses; Worst-case corner analysis; K-sigma statistical corner development; Design migration and centering mode for moving between process nodes; Cross test tuning to aid design centering; Global and local optimization modes; Reliability analysis
3.	**Simulation engine:** **The environment should provide for the following:** • Direct digital(Verilog) and analog(schematic) netlisting; Hierarchical editing with customized selection at each level; Direct netlisting of chosen hierarchy; Support for global design variables and global signals; Inherited connections **The simulator should be able to accept inputs in the following formats** • OpenAccess database; Verilog-AMS 2.0; VHDL-AMS 1076.1; Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions); VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000]); Spectre and SPICE netlist formats; SystemVerilog (IEEE 1800); Unified Power Format (UPF) or Common Power Format (CPF) **The simulator should support the following analog models** • Advanced-node models, including the latest versions of the BSIM CMG, BSIM IMG, and UTSOI models; MOSFET models, including the latest versions of the BSIM3, BSIM4, BSIM Bulk (BSIM6), PSP, and HiSIM; High-voltage MOS models, including the latest versions of the HiSIM HV, MOS9, MOS11, and EKV; Silicon-on-insulator (SOI), including latest versions of BTASOI, SSIMSOI, BSIMSOI, BSIMSOI PD, and HiSIM SOI; Bipolar junction transistor (BJT) models, including the latest versions of VBIC, HICUM, Mextram, HBT, and Gummel-Poon models; Diode models, including the diode, Phillips level 500, and CMC diode models; JFET models, including the JFET, Phillips level 100 JFET, and Individual dual-gate JFET models; IGBT models, including PSpice® IGBT model and HiSIM IGBT modelsResistors, including linear resistor, diffused resistor, CMC two-terminal and three-terminal resistor, and physical resistor models; GaAs MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov; GaN MESFET models, including Angelov, ASM, and MVSG models; Silicon TFT models, including RPI Poly-Silicon and Amorphous Silicon Thin-Film models; Verilog-A compact device models; Z and S domain sources; User-defined compiled model interface (CMI), allowing for the rapid inclusion of user-defined models; Josephson Junctions; Specialized reliability models (AgeMOS) for simulating the effect of HCI and BTI; Miscellaneous power models, including the relay, transformer, non-linear magnetic core, and winding; Miscellaneous RF models,

	including the dc block, dc feedthrough, and microstrip and stripline elements (bend, cross, corner, curve, open line, tee models) **The simulator should have support for the following netlisting options** • Spectre and SPICE netlist formats; Spectre, SPICE, and PSpice models; Verilog-A 2.0 LRM-compliant behavioral models and structural netlists; DSPF/SPEF parasitic formats; S-parameter data files in Touchstone, CITI-file, and Spectre formats; SST2, PSF, PSF XL, and FSDB waveform formats; Digital vector (VEC), Verilog-Value Change Dump (VCD), Extended Verilog-Value Change Dump (EVCD), and digital stimulus
4.	**Digital Synthesis:** **The synthesis platform should support the following:** • Parallel architecture that works seamlessly over multiple machines and multiple CPUs per machine; Automatic extraction of full timing and physical contexts for any subset of a design; Unified user interface with the Implementation System and Timing Signoff Solution; Physically aware logic structuring and mapping; Power domain and layer-aware net buffering; Single-pass multi-Vt optimization; Hierarchical RTL register clock gating; Timing-driven physically aware multi-bit flop mapping; Pipeline and general register retiming; Full support for multiple power domain design with automatic low-power cell insertion, both CPF and IEEE 1801 power-intent specifications supported; Concurrent MMMC timing analysis and optimization; Native integration of all design for test (DFT) logic insertion; Verilog 1995 and 2001, System Verilog 1800-2009, and VHDL 1987, 1993, and 2008 input formats; Verilog netlist and DEF placement output formats, Innovus database output format also supported • Multi-bit cell insertion to group registers for power and area reduction
5.	**Digital Implementation:** **The implementation should support the following:** • Massively parallel architectures for handling large designs and supporting multi-threading on multi-core workstations, as well as distributed processing over networks of computers; Placement technology, which is slack-driven and topology-, pin access-, and color-aware to provide optimal pipeline placement, wire length, utilization, and PPA; Advanced, multi-threaded, layer-aware optimization engine that is timing- and power-driven to reduce dynamic and leakage power; Unique concurrent clock and datapath optimization engine for better cross-corner variability and performance with reduced power; Slack-driven routing with track-aware timing optimization, which addresses signal integrity early on and improves post-route correlation; Full-flow multi-objective technology to support concurrent electrical and physical optimization; A customizable flow via a common UI and user commands across synthesis, implementation, and signoff with robust reporting and visualization
6.	**Platform:** • The suite should run on standard linux workstations as well as servers with support for multi-core and thread usage for simulation speedup.

General specifications:

a) Licensing period of 3 years.
b) Software installation and maintenance support for the duration of the license.
c) Should support redundant license servers.
d) The design and simulation suite should be able successfully handle the design database already present in the Integrated Circuits and Systems group at the Dept. of EE IIT Madras. **This is an important requirement for continuation of the research work within the group while reusing existing work and will be a deciding factor**.