DAC and ADC FMC cards: These cards will be used for sampling (and generating) the base band for a mm-wave system. These cards will be integrated with Xilinx FPGA boards.

DAC (Quantity 2)

1. Two channel DAC. Both channels should be synchronized.
2. Should support greater than 4 GSPS sampling rate (when both channels being used).
3. At least 14 bit resolution.
4. FMC (HPC) connectors for interface with Xilinx board VCU108
5. **Drivers and interface code for the card should be provided for Xilinx evaluation boards. Reference designs should be provided.**
6. Vita 57.1 compliant.
7. Standard connectors for interface with the analog signals.

ADC (Quantity 2)

1. Two channel ADC. Both channels should be synchronized.
2. Should support greater than 2 GSPS sampling rate. (When both channels are being used).
3. At least 10 bit resolution.
4. FMC (HPC) connectors for interface with the Xilinx board VCU108.
5. **Drivers and interface code for the card should be provided for Xilinx evaluation boards. Reference designs should be provided**.
6. Vita 57.1 compliant.
7. Standard connectors for interface with the analog signals.

- **The DAC and ADC should be provided with appropriate drivers for Xilinx FPGA boards with Vita 52 compliant FMC connectors.**
- **Documentation should be provided for the same.**

If applicable, the quotations should also include freight, insurance cost. The sealed quotations should be send to

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