	INDIAN INSTITUTE OF TECHNOLOGY MADRAS **Chennai 600 036** Telephone: [044] 2257 8368/9798 E-mail: tender@imail.iitm.ac.in	

The Senior Manager (Project Purchase) **Ref: ELE/2020/031/RADH/5G/MMWAVE**

Date: 16/11/2020

Open Tender No: ELE/2020/031/RADH/5G/MMWAVE

Due Date: 07/12/2020, 3 PM

Pre-Bid meeting: - NA

Technical Bid opening meeting on 07/12/2020, 4:00 PM at Department of Electrical Engineering, IIT-Madras.

Dear Sir/Madam,

On behalf of the Indian Institute of Technology Madras, offers are invited for the **Fabrication, BOM procurement and population of a Multiple Mmwave PCBs** conforming to the specifications given in Annexure I.

Vendor who can fabricate multilayer high-speed, RF PCBs and assemble the board need to respond to the tender.

For clarification contact: **CSD 400, Electrical sciences department IIT Madras Chennai – 600 036 Phone Number: 044-22578962.**

Instructions to the Bidder

I. **Preparation of Bids**: - The tenders should be submitted under two-bid system (i.e.,) Technical bid and Financial bid.

II. **Delivery of the tender**: - The tender shall be sent to the address mentioned below, either by post or by courier to reach our office before the due date and time specified in our schedule. The offer/bid can also be dropped in the tender box on or before the due date and time specified in the schedule.
The tender box is kept in the office of the:
The Senior Manager,
Project Purchase,
IC & SR Building 2nd floor,
I.I.T. Madras,
Chennai – 600 036

III. **Opening of the tender**: - The offer/bids will be opened by a committee duly constituted for this purpose. The technical bids will be opened first and will be examined by a technical committee which will decide the suitability of the bids as per our specifications and requirements. All bidders will be invited for opening of the technical bids. For opening the financial bid, only technically qualified bidders will be called.

IV. **Prices**: - The price should be quoted in net per unit (after breakup) and must include all packing and delivery charges to the **Department of Electrical Engineering**. The offer/bid should be exclusive of taxes and duties. The percentage of tax & duties should be clearly indicated separately. Kindly note that IIT Madras is eligible for concessional GST and relevant certificate will be issued.

In case of import supply, the price should be quoted without custom duty. IIT Madras is exempted from levy of IGST on Imports and eligible for concessional custom duty (not exceeding 5%) and the price should be quoted on EX WORKS and CIP basis (stating the Cost, Insurance, Freight separately) and indicating the mode of shipment.

V. **Agency Commission:** - Agency commission, if any, will be paid to the Indian agents in rupees after receipt of the equipment and its satisfactory installation. Agency Commission will not be paid in foreign currency under any circumstances. The details should be explicitly shown in the tender document even in the case of 'Nil' commission. The tenderer should indicate the percentage of agency commission to be paid to the Indian agent. The Foreign Principal should indicate the percentage of payment and it should be included in the basic price quoted originally (if any).

VI. **Terms of Delivery:** - The item should be supplied to the **Department of Electrical Engineering**, **IIT Madras** as per the Purchase Order. In case of import supply, the item should be delivered at the cost of the supplier to our Institution. The Installation/Commissioning should be completed as specified in our important conditions.

VII. The ultimate customer (5G Testbed team) will be doing a final inspection for the product and shall reject the material/product at the cost of the supplier in case of a quality/specification complaint. The rejected goods are to be removed from the supply point at the expense of the supplier and materials should be replaced within the time limit as intimated by the 5G Testbed team.

VIII. Defects if any, noticed within 12 months from the date of completion, will be rectified by the bidder.

IX. **Technical Bid Opening**: The technical bid will be opened on **07/12/2020, 4 PM** at the **Department of Electrical Engineering, IIT-Madras**. The financial bids of those tenderers who are technically qualified will be opened at a later date under intimation to them.

X. IIT Madras reserves the full right to accept / reject any tender at any stage without assigning any reason.

Yours sincerely,

The Senior Manager (Project Purchase)
IC&SR Building, I.I.T. Madras,
Chennai – 600 036.

SCHEDULE

Important Conditions of the tender

1. The due date for the submission of the tender is **07/12/2020, 3 PM.** Tenders received after the due date will not be considered.

2. The offers / bids should be submitted under two bid system (i.e.) Technical bid and financial bid. The Technical bid should consist of all technical details / specifications only. The Financial bid should indicate item-wise price for each item, and it should contain all Commercial Terms and Conditions including Taxes, transportation, packing & forwarding, installation, guarantee, payment terms, pricing terms etc. The Technical bid and financial bid should be put in separate covers and sealed. Both the sealed covers should be put in a bigger cover. The Open Tender for supply of **"Fabrication, BOM procurement and population of a Multiple Mmwave PCBs"** should be written on the left side of the Outer bigger cover and sealed.

3. **EMD: - The EMD (Should be in INR) in the form of Account Payee Demand Draft / Banker's Cheque for Rs. 2,00,000 (INR); drawn in favor of The Registrar-IIT Madras, payable at Chennai should be enclosed in the cover containing Technical bid.** Any offer not accompanied with the EMD shall be rejected summarily as non-responsive.

   The EMD of the unsuccessful bidders shall be returned within 30 days of the end of the bid validity period. The same shall be forfeited, if the tenderers withdraw their offer after the opening during the bid validity period. The Institute shall not be liable for payment of any interest on EMD. EMD is exempted for Micro and Small Enterprises (MSE) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME) and Startups as recognized by Department of Industrial Policy & Promotion (DIPP).

   When a foreign vendor does not have a local agent in India, he can submit a demand draft equal to **Rs. 200,000 (INR)** ***or wire transfer the amount to our account as detailed in the attachment (Annexure II) and enclose the proof with the technical bid.***

4. **Performance Security: -** The successful bidder should submit Performance Security for an amount of 5% of the value of the contract/supply. The Performance Security may be furnished in the form of an Account Payee DD, FD Receipt from the commercial bank, Bank Guarantee from any nationalized bank in India. **The performance security should be furnished within 14 days from the delivery of the purchase order.**

   Performance Security in the form of Bank Guarantee: - In case the successful bidder wishes to submit Performance Security in the form of Bank Guarantee, the Bank Guarantee should be routed through the Beneficiary Bank to the end user bank. Otherwise, the Indian Agent of the foreign vendor has to submit a Bank Guarantee from a Nationalized Bank of India.
   The Bank Guarantee should remain valid for a period of sixty days beyond the date of completion of all contractual obligations of the supplier including the warranty obligations.

5. **Indian agent:** If an Indian agent is involved, the following documents must be enclosed:

Foreign principal's proforma invoice indicating the commission payable to the Indian Agent and nature of after-sales service to be rendered by the Indian Agent.

- ✓ Copy of the agency agreement with the foreign principal and the precise relationship between them and their mutual interest in the business.

6. Original catalogue (not any photocopy) of the quoted model duly signed by the principals must accompany the quotation in the Technical bid.

7. Compliance or Confirmation report with reference to the specifications and other terms & conditions should also be obtained from the principal.

8. **Validity:** The validity of Quotation should not be less than 90 days from the due date of tender.

9. **Delivery Schedule**: - The tenderer should indicate clearly the time required for delivery of the item (subjected to the executive committee-IIT Madras approval). In case there is any deviation in the delivery schedule, liquidated damages clause will be enforced or penalty for the delayed supply period will be levied.

   If there is delay, the penalty will be @1% per week of delay subject to a max of 10% of the value of purchase order and if the delay is more than accepted time frame by IITM, the PO would be cancelled, and liquidated damages will be enforced.

10. **Risk Purchase Clause**: - In the event of failure of supply of the item/equipment within the stipulated delivery schedule, the purchaser has all the right to purchase the item/equipment from other sources on the total risk of the supplier under risk purchase clause.

11. **Payment**: -
    (i) No Advance payment will be made for Indigenous purchase. The payment is based on the schedule provided in Annexure 1.

12. **On-site Installation**: - The equipment or machinery has to be installed or commissioned by the successful bidder within number of days (as prescribed by PI) from the date of receipt of the item at site of IIT Madras

13. **Warranty/Guarantee**: - The offer should clearly specify the warranty or guarantee period for the machinery/equipment. Any extended warranty offered for the same has to be mentioned separately (For more details please refer our Technical Specifications).

14. **Late offer**: - The offers received after the due date and time will not be considered. The Institute shall not be responsible for the late receipt of Tender on account of Postal, Courier or any other delay.

15. **Acceptance and Rejection**: - I.I.T. Madras has the right to accept the whole or any part of the Tender or portion of the quantity offered or reject it in full without assigning any reason.

16. **Do not quote the optional items or additional items unless otherwise mentioned in the Tender documents / Specifications.**

17. Disputes and Jurisdiction:

Settlement of Disputes: Any dispute, controversy or claim arising out of or in connection with this PO including any question regarding its existence, validity, breach or termination, shall in the first instance be attempted to be resolved amicably by both the Parties. If attempts for such amicable resolution fails or no decision is reached within 30 days whichever is earlier, then such disputes shall be settled by arbitration in accordance with the Arbitration and Conciliation Act, 1996. Unless the Parties agree on a sole arbitrator, within 30 days from the receipt of a written request by one Party from the other Party to so agree, the arbitral panel shall comprise of three arbitrators. In that event, the supplier will nominate one arbitrator and the Project Coordinator of IITM shall nominate on arbitrator. The Dean IC&SR will nominate the Presiding Arbitrator of the arbitral tribunal. The arbitration proceeding shall be carried out in English language. The cost of arbitration and fees of the arbitrator(s) shall be shared equally by the Parties. The seat of arbitration shall be at IC&SR IIT Madras, Chennai.

a. **The Applicable Law:** This Purchase Order shall be construed, Interpreted and governed by the Laws of India, Court at Chennai shall have exclusive jurisdiction subject to the arbitration clause.
b. Any legal disputes arising out of any breach of contact pertaining to this tender shall be settled in the court of competent jurisdiction located within the city of Chennai in Tamil Nadu.

18. All Amendments, time extension, clarifications etc., will be uploaded on the website only and will not be published in newspapers. Bidders should regularly visit the above website to keep themselves updated. No extension in the bid due date/ time shall be considered on account of delay in receipt of any document by mail.

Acknowledgement: - It is hereby acknowledged that the tenderer has gone through all the conditions mentioned above and agrees to abide by them.

SIGNATURE OF TENDERER
ALONG WITH SEAL OF THE
COMPANY WITH DATE

Annexure I

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1 General Technical Specifications, quantities for compliance

This tender is about manufacture of RF boards. The details of the RF boards are specified below. We request the bidder to go through these carefully and provide **compliance tables for the following**

1. The general compliance terms in the Compliance terms Section 1.2
2. Technical compliance tables: For each board in ***Table 1***, please provide compliance **(individually)** for
    1. Each requirement for PCB manufacturing, stackup, via requirements and impedance requirements (As per sections provided for each board)

Mmwave array 26GHz	Section 2
Mmwave array 28GHz	Section 3
Mmwave RF RRH	Section 4
Mmwave RF UE	Section 5
Mmwave connector board	Section 6

    2. Capability for Assembly and X-Ray inspection for all the above boards as per the details provided in each section.

Hence, each tender bid in its technical part should be accompanied by 11 compliance tables, once for the general compliance provided in Section 1.2, five PCB fabrication compliance tables and five PCB assembly compliance tables.

1.1 Quantities and schedule of each board

There are two stages in the fabrication:

Stage1: Some boards (as specified in next table) should be manufactured and assembled for testing. Once the manufacturing and assembly is tested and approved by IITM, for each board, the vendor should proceed to the second stage.

Stage2: The other boards (as specified in next table) should be manufactured and assembled. The boards in stage 2 might be some modified (based on testing stage 1) version of stage1 boards.

Table 1: Boards being manufacture and the quantities

Board name	Overall Quantity required	Stage1	Stage 2
Mmwave array 26GHz	10	1	9
Mmwave array 28GHz	6	1	5
Mmwave RF RRH	10	1	9
Mmwave RF UE	10	1	9
Mmwave connector board	10	1	9

Stage 1: Delivery timeline is 3 weeks from day of the PO and the provision of PCB Gerber's by IITM. This includes all the time including the engineering questions and clarifications.

Stage 2: Delivery timeline of each board in stage 2 is 4 weeks from the day of the approval of Stage2 for that particular board. The approval time for individual boards might vary and be staggered (because of testing).

- The delivery time cannot be changed.
- All the boards have to be quoted.
- The stack up, PCB pre-peg materials of the boards, the via dimensions and any technical specifications of these boards were designed after extensive simulations and will be difficult to change.
- Basic rework might be requested (as required) and the vendor should support this without any additional cost
- The technical details of the PCB Fabrication, BOM details and PCB assembly for each board are provide below.
- The exact BOM details (excel sheet of BOM) can be obtained by emailing rganti@ee.iitm.ac.in, lakshman@5gtbiitm.in and tender@imail.iitm.ac.in after providing details about your manufacturing capabilities. You might be requested to sign an NDA for the same before any technical documentation can be provided.

1.2 Compliance terms

Please provide an explicit compliance table for all the points below with justification as applicable.

a. The bidding firm should have existed for at least 5 years
b. The bidding firm should have a turnover of at least 10 crores INR. Documentation for the same has to be provided.

c. Please indicate prior RF and high-density boards (of similar complexity of at least 12 layers) that you have fabricated. Vendors without prior experience (of at least 5 prior boards) of similar complexity may be disqualified. Documentary evidence of the same should be provided.
    i. Should have fabricated and assembled boards with date rates support up to 100 Gbps or RF boards above 25 GHz. Evidence for the same should be provided
d. The firm should quote for all the boards, the details of which are provided in the next section.
e. Capability for DFA and DFF reports
f. The vendor should have inhouse design capability to modify the layout and do SI analysis of the board after the 1st run as required. Details about this design capability should be provided.
g. Explicitly indicate the PCB Fab details and **its technical capabilities**, where each board will be fabricated.
    i. References to online material/documentation for verification **should** be provided. The bid might be disqualified if the technical capabilities of the proposed FAB are not clear or do not meet the technical requirements of the boards.
    ii. Prior engineering compliance with the FAB (for meeting the technical specifications, as mentioned in the subsequent sections) for manufacturing the required PCB should be provided (for each PCB) in the templates provided in the next sections.
        - The confirmation from the FAB (as email exchange or letters (in English)) should also be provided in the tender.
        - Some important considerations
            a. Most of the boards require blind vias.
            b. Impedance control is required for some boards.
            c. Rogers material is used for laminate and pre-preg for many boards
    iii. The country of the FAB should explicitly be mentioned.
        - If these boards are manufactured in countries that share a land border with India, the bid will be eligible only if the FAB is registered with the competent authority and the required approvals are obtained as mentioned in the GFR amendments (Rule 144 (xi)) posted on 23rd July 2020.
        - These required approvals have to be part of the technical tender for the bid to be valid.
h. Explicitly indicate the plant details **and its technical capabilities**, where the board will be assembled.

i. Please indicate the country of the assembly facility. **The assembly facility should be in India**.
    - Where IITM can ship the required components (FPGA's, ICs, Transceivers)
    - The assembly plant and testing facility should be in India and should be ready for some basic rework as the case arises without additional cost

ii. Support for double-sided PCB assembly

iii. Have at least five SMT assembly lines which can do complex PCB assemblies. pictures/evidence for the same should be provided.

iv. Assembly should have the capability of IPC-610 class2 and class 3 standards

v. The assembly line should be capable of handling 01005 discrete components, 0.4 mm BGA's, 0.4 mm pitch, LGA CC-20-3, and should have the capability of odd angle placement

vi. Should have the facility for flying probe testers and automated optical lines (inspection)

vii. In house X-ray inspection should be available

i. Agreement to the stage 1 and stage 2 manufacturing along with the quantities provided in previous section

j. Agreement to the payment schedule provided below.

k. Compliance to the time schedule provided below Table 1. The time schedule cannot be relaxed and is inclusive of all engineering questions and clarifications and shipment.

l. The BOM (available as excel sheets upon request) has to be procured for the required quantities by the vendor for the assembly.

Payment schedule (Please confirm your compliance)

- 50% of the total cost will be paid after successful completion of stage 1.
- 50% of the total cost will be paid after successful completion of stage 2.

- If the Stage1/Stage2 fabrication is not to the specifications, or manufacturing defects are observed, or undue delays happen, IITM reserves the right to cancel the PO without any payment to the vendor.

The PCB Fabrication cost, BOM cost and Assembly cost should be separated and be explicitly mentioned for each board separately in the financial bid.

The final evaluation will be based on L1 price for the technically qualified bids.

2 Mmwave array 26GHz

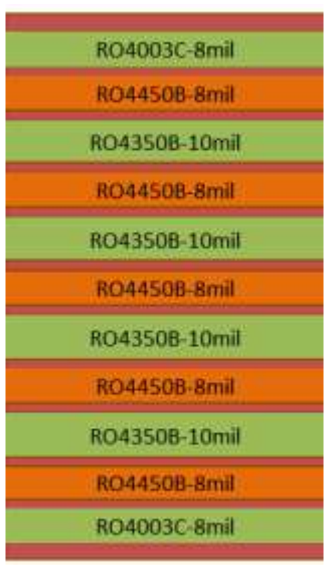
2.1 PCB fabrication Specification

In this table (See section 1), please indicate if you will be able to handle the required specification.

Description	Specification	Compliance Yes/No
No. of layers	12	
Via Technology	Mechanical Through Hole vias and mechanical blind vias from L1-L2, L1-L4, L1-L6, L1-L8, L1-L10	
Material (Specify clearly whether High Tg or Normal Tg)	RO4003C – 8mil (2-Nos) RO4450F – 8mil (5-Nos) RO4350B – 10mil (4-Nos) (Image provided below)	
Impedance control (Yes/No) Mention tolerance	No	
Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 1. 2.43mm thickness over the laminate 2. Tolerance 5%	
Copper finish (35 microns/70 microns/ any other)	Copper Thickness: TOP Layer(L1): Signal layer thickness 35um BOTTOM layer (L12): Signal layer thickness 35um INNER Layers (L2-L11): Signal layer Thickness 18um	
Min. finished hole dia (mm)	0.2 mm	
Min. trace width (mm)	0.1mm	
Min. spacing (mm)	0.1mm	
Min. Annular ring (mm)	0.1 mm	
Board finish (Hot Air Leveled/ electro less Ni-Au / Hard Gold / any other)	Gold plating without nickel (3um) preferred or ISIG	
PCB Dimension in mm	Overall Board size is L X W = 120mm X 113mm.	
Metal core board	No	
Mil Grade	No	
Whether Group B Test Report required	No	
Solder Mask Color	Green	
Silkscreen Color	White	

RoHS Complaint	Yes	
UL Logo Required	No	
Back Drilling Required	No	
RF VIAS	Yes	
X-Ray Inspection required	Yes	
Via filling	Yes; **Non-conductive** filling.	
Via sizes and configuration	See Section 2.2.1	
Stackup as per Section	See Section 2.2	
DFF and DFA report to be done	Yes	

2.2 Stackup Specifications



2.2.1 VIA details

Approximate number of via’s

1. L1-L12 (PTH): 600
2. L1-L2 (blind vias): 4000
3. L1-L4 (blind vias): 300
4. L1-L6 (blind vias): 1000
5. L1-L8 (blind vias): 500
6. L1-L10(blind vias): 1700

2.3 Assembly

1. BOM will be provided as an excel sheet at request
2. Assembly schedule of the board
    a. Components should be procured as per the BOM provided.

In this table (See section 1), please indicate if you will be able to handle the required specification.

Description	Specification	Compliance Yes/No
No of comps per board	750	
No of BGAs per board	64	
Maximum pin count	56 bumps, 0.4 mm BGA	
Minimum BGA pitch	0.4 mm	
Total No of points to be soldered (no of pins)	5000 (approx.)	
PTH pins	Nil	
Both side assembly	Single side	
Board Size	120 X 113 mm	
Board Thickness	2.43 mm over laminate	
No of Layers	12	
X-ray verification of the assembled boards	Yes. Test results should be provided.	

3 Mmwave array 28GHz

3.1 PCB Fabrication Specification

In this table (See section 1), please indicate if you will be able to handle the required specification

Description	Specification	Compliance Yes/No
No. of layers	10	
Via Technology	Mechanical Through Hole vias and mechanical blind vias from L1-L2, L1-L6,	

	L1-L8	
Material (Specify clearly whether High Tg or Normal Tg)	R04003C – 8mil (2-Nos) R04450F – 8mil (4-Nos) R04350B – 10mil (3-Nos) (Image provided below)	
Impedance control (Yes/No) Mention tolerance	No	
Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 1. 1.98mm thickness over the laminate 2. 2.19mm thickness over copper 3. Tolerance 5%	
Copper finish (35 microns/70 microns/ any other)	Copper Thickness: TOP Layer(L1): Signal layer thickness 35um BOTTOM layer (L10): Signal layer thickness 35um INNER Layers (L2-L9): Signal layer Thickness 18um	
Min. finished hole dia (mm)	0.2 mm	
Min. trace width (mm)	0.1 mm	
Min. spacing (mm)	0.1 mm	
Min. Annular ring (mm)	0.1 mm	
Board finish (Hot Air Leveled/ electro less Ni-Au / Hard Gold / any other)	Gold plating without nickel (3um) preferred or ISIG	
PCB Dimension in mm	Overall Board size is L X W = 70mm X 73mm.	
Metal core board	No	
Mil Grade	No	
Whether Group B Test Report required	No	
Solder Mask Color	Green	
Silkscreen Color	White	
RoHS Complaint	Yes	
UL Logo Required	No	
Back Drilling Required	No	
RF VIAS	Yes	
X-Ray Inspection required	Yes	
Via filling	Yes; **Non-conductive** filling.	

Via sizes and configuration	See Section 3.2.1	
Stackup as per Section	See Section 3.2	
DFF and DFA report to be done	Yes	

3.2 Stack up Specifications

RO4003C-8mil
RO4450B-8mil
RO4350B-10mil
RO4450B-8mil
RO4350B-10mil
RO4450B-8mil
RO4350B-10mil
RO4450B-8mil
RO4003C-8mil

3.2.1 VIA details

Approximate number of vias

1. L1-L10(PTH): 300
2. L1-L2 (blind vias): 1250
3. L1-L6 (blind vias): 500
4. L1-L8(blind vias): 600

3.3 Assembly

1. BOM will be provided as excel sheet.

In this table (See section 1), please indicate if you will be able to handle the required specification.

Description	Specification	Compliance Yes/No
No of comps per board	500	
No of BGAs per board	16	
Maximum pin count	56 bumps, 0.4 mm BGA	
Minimum BGA pitch	0.4 mm	

Total No of points to be soldered (no of Pins)	2000(approx.)	
PTH pins	Nil	
Both side assembly	Single side	
Board Size	70 X 73 mm	
Board Thickness	2.19mm over copper	
No of Layers	10	
X-ray verification of the assembled board	Yes. Test results should be provided.	

4 Mmwave RF RRH

4.1 PCB Fabrication Specification

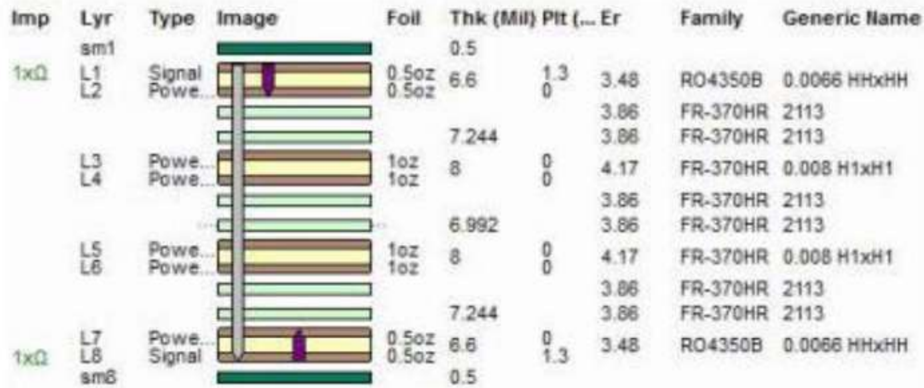
In this table (See section 1), please indicate if you will be able to handle the required specification

Description	Specification	Compliance Yes/No
No. of layers	8	
Via Technology	Mechanical Through Hole & Mechanical Blind vias from layers L1-L2 & L8-L7.	
Material	RO4350B & 370HR	
Impedance control (Yes/No) Mention tolerance	Yes	
Board thickness (2mm) Mention Tolerance	Entire board must be: 1. 68.6 mil thickness over the copper 2. 69.6 mil thickness over the Solder-mask	
Copper finish (35 microns/70 microns/ any other)	Copper Thickness: • Outer Layers:	

	• Signal Layer Thickness 2.067 mils • Inner Layers: • Power and signal layers 2.756 mils • GND layer 1.378 mils	
Min. finished hole dia (mil)	8 mil Mechanical drill	
Min. trace width (mil)	8 mil	
Min. spacing (mil)	• Outer Layers: 5 mil • Inner Layers: 7 mil	
Min. Annular ring (mil)	8 mil drill (inner diameter) 5 mil annular ring width.	
Board finish (Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	ISIG	
PCB Dimension in mm	202 X 65 mm	
Metal core board	No	
Mil Grade	No	
Whether Group B Test Report required	No	
Solder Mask Color	Green	
Silkscreen Color	White	
RoHS Compliant	No	
UL Logo Required	Yes	
Via Filling Required	**No**	
Stackup requirements	See Section 4.2	
Impedance requirements	See Section 4.2.1	
DFF and DFA report to be done	Yes	

4.2 Stackup Specifications

<u>Stack up requirements of the board (*Material and Stack-up cannot be changed*.</u>



Imp	Lyr	Type	Image	Foil	Thk (Mil)	Plt (...	Er	Family	Generic Name
	sm1				0.5				
1xΩ	L1 L2	Signal Powe...		0.5oz 0.5oz	6.6	1.3 0	3.48	RO4350B	0.0066 HHxHH
							3.86	FR-370HR	2113
					7.244		3.86	FR-370HR	2113
	L3 L4	Powe... Powe...		1oz 1oz	8	0 0	4.17	FR-370HR	0.008 H1xH1
							3.86	FR-370HR	2113
					6.992		3.86	FR-370HR	2113
	L5 L6	Powe... Powe...		1oz 1oz	8	0 0	4.17	FR-370HR	0.008 H1xH1
							3.86	FR-370HR	2113
					7.244		3.86	FR-370HR	2113
1xΩ	L7 L8	Powe... Signal		0.5oz 0.5oz	6.6	0 1.3	3.48	RO4350B	0.0066 HHxHH
	sm8				0.5				

Impedance Table

Index	Layer	Required Impedance [ohms]	Tol [ohms] +/-	Type	Ref 1	Ref 2	Orig LW [mil]	Orig Spacing [mil]	Orig CP Spacing [mil]	Finished LW [mil]	Finished Spacing [mil]	Fin. CP Spacing [mil]	Impedance Simulation [ohms]	Impedance before Mask [ohms]	IMG
a	1	50	5	CP SE Uncoated		2	11.81		6.70	11.81		6.70	49.8		
b	8	50	5	CP SE Uncoated		7	11.81		6.70	11.81		6.70	49.8		

Customer required thickness	69.6 +/- 6 mils Measured: Over mask on plated copper

4.2.1 Impedance Requirements

Layer	Structure Type	Target Impedance (OHMs)	Tolerance	Reference Layer	Target Linewidth (mm)	Coplanar Clearance (mm)
1,8	Coplanar Single Ended	50	+/- 10 %	2,7	0.3	0.174

4.3 Assembly

- The BOM (As specified in the excel sheets) has to **be procured by the vendor.**

Description	Specification	Compliance Yes/No
No of comps per board	1515	
Maximum pin count	61, QFN	
Minimum pitch	0.4 mm	
Total No of points to be soldered (no of Pins)	4835(approx.)	
PTH pins	2500 (approx.)	
Both side assembly	Yes	

Board Size-	202 X 65 mm	
Board Thickness	69.6 Mils	
No of Layers	8	
X-ray verification of the board	Yes. Test results should be provided.	

5 Mmwave RF UE

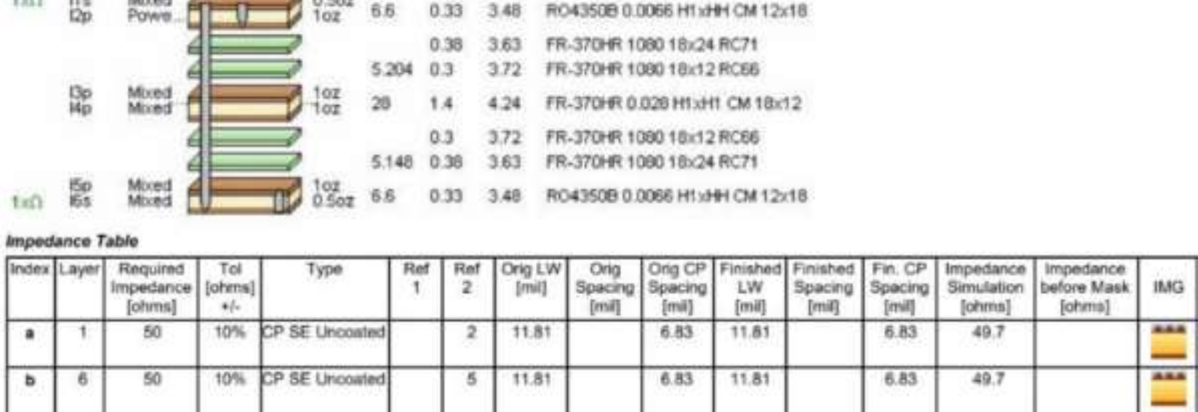
5.1 PCB Fabrication Specification

Description	Specification	Compliance Yes/No
No. of layers	6	
Via Technology	Mechanical Through Hole & Mechanical Blind vias from layers L1-L2 & L6-L5.	
Material	RO4350B & 370HR	
Impedance control (Yes/No) Mention tolerance	Yes	
Board thickness (2mm) Mention Tolerance	Entire board must be: • 66.7 mil thickness over the copper • 67.7 mil thickness over the Solder-mask	
Copper finish (35 microns/70 microns/ any other)	Copper Thickness: • Outer Layers: • Signal Layer Thickness 2.067 mils • Inner Layers: • Power and signal layers 2.756 mils • GND layer 2.756 mils	
Min. finished hole dia (mil)	8 mil Mech	

Min. trace width (mil)	8	
Min. spacing (mil)	• Outer Layers: 5 mil • Inner Layers: 7 mil	
Min. Annular ring (mil)	8 mil drill (inner diameter) 5 mil annular ring width.	
Board finish (Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	ISIG	
PCB Dimension in mm	180 X 100	
Metal core board	No	
Mil Grade	No	
Whether Group B Test Report required	No	
Solder Mask Color	Green	
Silkscreen Color	White	
RoHS Compliant	No	
UL Logo Required	Yes	
Via Filling Required	**No**	
Stackup requirements	See Section 5.2	
Impedance requirements	See Section 5.2.1	
DFF and DFA report to be done	Yes	

5.2 Stackup Specifications

Stack up requirements of the board (*Material and Stack-up cannot be changed*.)



Imp	Lyr	Type	Foil	Thk (...	Tol (Mi...		Name
1xΩ	l1s l2p	Mixed Powe...	0.5oz 1oz	6.6	0.33	3.48	RO4350B 0.0066 H1xHH CM 12x18
					0.38	3.63	FR-370HR 1080 18x24 RC71
				5.204	0.3	3.72	FR-370HR 1080 18x12 RC66
	l3p l4p	Mixed Mixed	1oz 1oz	28	1.4	4.24	FR-370HR 0.028 H1xH1 CM 18x12
					0.3	3.72	FR-370HR 1080 18x12 RC66
				5.148	0.38	3.63	FR-370HR 1080 18x24 RC71
1xΩ	l5p l6s	Mixed Mixed	1oz 0.5oz	6.6	0.33	3.48	RO4350B 0.0066 H1xHH CM 12x18

Impedance Table

Index	Layer	Required Impedance [ohms]	Tol [ohms] +/-	Type	Ref 1	Ref 2	Orig LW [mil]	Orig Spacing [mil]	Orig CP Spacing [mil]	Finished LW [mil]	Finished Spacing [mil]	Fin. CP Spacing [mil]	Impedance Simulation [ohms]	Impedance before Mask [ohms]	IMG
a	1	50	10%	CP SE Uncoated		2	11.81		6.83	11.81		6.83	49.7		
b	6	50	10%	CP SE Uncoated		5	11.81		6.83	11.81		6.83	49.7		

Customer required thickness	67.7 +/- 6 mils Measured: Over mask on plated copper

5.2.1 Impedance Requirements

Layer	Structure Type	Target Impedance (OHMs)	Tolerance	Reference Layer	Target Linewidth (mm)	Coplanar Clearance (mm)
1,6	Coplanar Single Ended	50	+/- 10 %	2,5	0.3	0.174

5.3 Assembly

FR2_AFE Board

Description	Specification	Compliance Yes/No
No of comps per board	450 (approx.)	
Maximum pin count	61, QFN	
Minimum pitch	0.4 mm	
Total No of points to be soldered (no of Pins)	1700 (approx.)	
PTH pins	1000 (approx.)	
Both side assembly	Yes	
Board Size	180 X 100 mm	
Board Thickness	67.7 Mils	
No of Layers	6	
X-ray verification of the board	Yes. Test results should be provided.	

6 Mmwave connector board

6.1 PCB Fabrication Specification

<u>Stack up requirements of the board (*Material and Stack-up cannot be changed*.)</u>

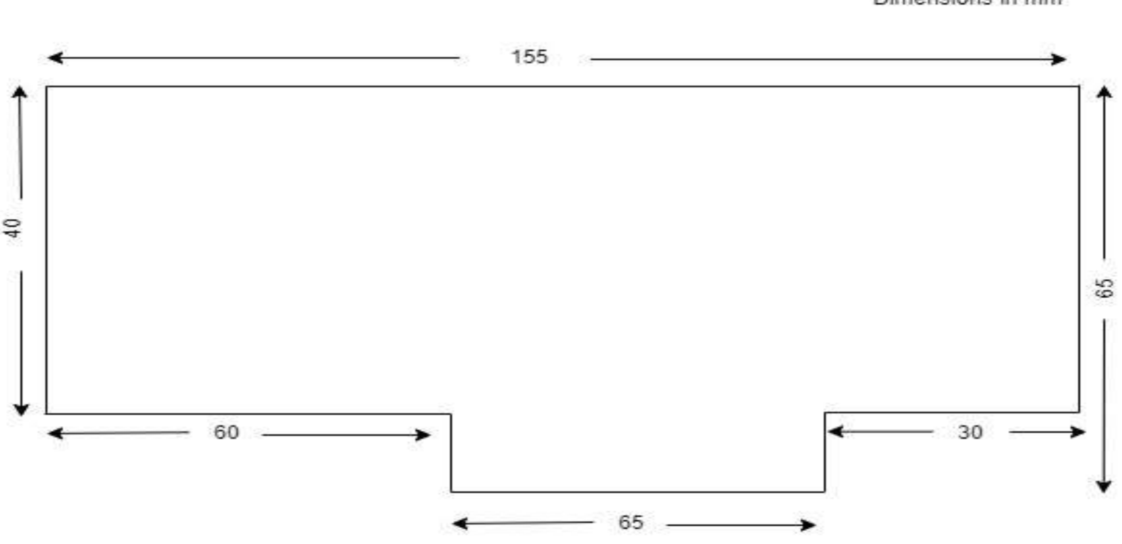
Description	**Specification**	**Compliance Yes/No**
No. of layers	6	
Via Technology	Through Hole with filled via option	
Material	370HR	
Impedance control (Yes/No) Mention tolerance	Yes	
Board thickness (1.6mm) Mention Tolerance	Entire board must be: • 61.226mil thickness over the copper • 65.226mil thickness over the Solder-mask	

Copper finish (12 microns)	Copper Thickness:
	• Outer Layers:
	    • Signal Layer Thickness 1.85 mil
	• Inner Layers:
	    • Power and GND layer 1.26 mil
	    • Signal layer 0.689 mil	

Min. finished hole dia (mil)	8 Mil Mech	
Min. trace width (mil)	4	
Min. spacing (mil)	4	
Min. Annular ring (mil)	8 mil drill (inner diameter) 4 mil annular ring width. Annular ring size Drill size	

Board finish (Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Gold finish	
PCB Dimension in mm	Refer below image	
Metal core board	No	
Mil Grade	No	
Whether Group B Test Report required	No	
Solder Mask Color	Green	
Silkscreen Color	White	
RoHS Compliant	No	
UL Logo Required	Yes	
Via Filling Required	Yes; **non-conductive** filling.	
RF Vias	No	
PCB dimension	See Section 6.1.1	
Stackup requirements	See Section 6.2	
Impedance requirements	See Section 6.2.1	

6.1.1 PCB Dimension



6.2 Stackup Specifications

Layer	Stack up	Description	Type	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000BN GREEN	SolderMask	2.000			3.900	
1		Copper Foil 12 microns	Copper	1.850		100.000		1, 2, 3
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.198	4.396		3.540	
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.198	-		3.540	
2				1.260		60.000		
		Isola 370HR 4 mil core 1/H (1-2116)	FR4	4.000	4.000		4.170	
3				0.689		30.000		4, 5, 6
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.209	36.835		3.540	
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.209	-		3.540	
		Isola 370HR 28 mil core H/H	FR4	28.000	-		4.240	
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.209	-		3.540	
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.209	-		3.540	
4				0.689		30.000		7, 8, 9
		Isola 370HR 4 mil core H/1 (1-2116)	FR4	4.000	4.000		4.170	
5				1.260		60.000		
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.198	4.396		3.540	
		Isola 370HR Prepreg 106 RC76 - German	Dielectric	2.198	-		3.540	
6		Copper Foil 12 microns	Copper	1.850		100.000		10, 11, 12
		Taiyo PSR 4000BN GREEN	SolderMask	2.000			3.900	

Copper Thickness = 7.598 | Dielectric Thickness = 53.628 | Solder Mask Thickness = 4.000 | Stack Up Thickness = 61.226 | Stack Up Thickness with Soldermask = 65.226

6.2.1 Impedance Requirements

Impe-dance ID	Layer	Structure Type	Target Impedance (Ohm)	Reference Layer	Target Line width (mil)	Trace Separation (mil)	Tol. (+/- %)
1	1	Coated Microstrip 1B	50.02	2	7.56	0.00	10.00
2	1	Edge coupled coated Microstrip 1B	90.14	2	6.3	6.00	10.00
3	1	Edge coupled coated Microstrip 1B	100.13	2	5	6.50	10.00
4	3	Offset strip line 1B1A	50.01	2	5.418	0.00	10.00
5	3	Edge coupled offset strip line 1B1A	90.1	2	5	6.50	10.00
6	3	Edge coupled offset strip line 1B1A	100.19	2	4	7.10	10.00
7	4	Offset strip line 1B1A	50.01	5	5.418	0.00	10.00
8	4	Edge coupled offset strip line 1B1A	90.1	5	5	6.50	10.00
9	4	Edge coupled offset strip line 1B1A	100.19	5	4	7.10	10.00
10	6	Coated Microstrip 1B	50.02	5	7.56	0.00	10.00

11	6	Edge coupled coated Microstrip 1B	90.14	5	6.3	6.00	10.00
12	6	Edge coupled coated Microstrip 1B	100.13	5	5	6.50	10.00

6.3 Assembly

mmWave_interface_V2 Board

Description	**Specification**	**Compliance Yes/No**
No of comps per board	400	
Maximum pin count	48, SOP	
Minimum pitch	15 mil	
Total No of points to be soldered (no of Pins)	1000 (approx.)	
PTH pins	50 (approx.)	
Both side assembly	Yes	
Board Size-	Refer dimension image in Section 6.1.1.	
Board Thickness	1.6 mm	
No of Layers	6	
X-ray verification of the board	No	

CENTRE FOR INDUSTRIAL CONSULTANCY & SPONSORED RESEARCH (IC&SR)
INDIAN INSTITUTE OF TECHNOLOGY MADRAS
CHENNAI 600 036

ELECTRONIC CLEARING SERVICE (Credit Clearing)/ REAL TIME GROSS SETTLEMENT (RTGS) FACILITY FOR RECEIVING PAYMENTS

A. Details of Account Holder

Name of the Institution	Indian Institute of Technology - Madras
Complete Contact Address	Industrial Consultancy and Sponsored Research Indian Institute of Technology-Madras, IIT- Madras Campus Post Office, Sardar Patel Road, Guindy, CHENNAI - 600 036
Telephone No./ Fax No.	Tel - 044-22578355 / Fax - 044-22570545
E- mail ID of the FO/AO/REG/DIR	dricsr@iitm.ac.in

B. Bank Account Details:

Institution Account Name (As per Bank Record)	The Registrar, Indian Institute of Technology - Madras
Account No.	2722101001741
Account Print Name	IIT F A/C , The Registrar IIT Madras
IFSC CODE	CNRB0002722
Bank Name (in full)	Canara Bank
Branch Name	IIT-Madras Branch
Complete Branch Address	Canara Bank, IIT-Madras Branch, IIT- Madras Campus Post Office, Sardar Patel Road, Guindy, CHENNAI - 600 036
MICR No.	600015085
Account Type	Savings Account

Certified that the Institute's account is in an RTGS enabled branch.
I hereby declare that the particulars given above are correct and complete.

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IC & SR, I.I.T. MADRAS
CHENNAI - 600 036

Certified that the particulars furnished above are correct as per our records.

Date:

For CANARA BANK
SENIOR MANAGER
I.I.T. CHENNAI 600 036.

Signature of the Authorized Bank Official with Bank Seal.

B. SEKAR
Senior Manager
SP No. 39312

Phone : +91 (0) 44 2257 8062 / 8061 / 8060 Fax : +91 (0) 44 2257 0545 / 2257 8366 email : deanicsr@iitm.ac.in website : http://www.iitm.ac.in

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INDIAN INSTITUTE OF TECHNOLOGY MADRAS
CHENNAI 600 036

K VIJAYALAKSHMI
DEPUTY REGISTRAR (IC&SR) i/c

Project Accounts
July 5, 2019

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FOR TRANSFER OF CURRENCY US DOLLAR

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For credit to

USD ACCOUNT No: 001 – 1395969, of CANARA BANK INTERNATIONAL DIVISION MUMBAI

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This is to certify that particulars furnished are correct.

For CANARA BANK

Senior Manager
Canara Bank – IIT Madras branch

B. SEKAR
Senior Manager
SP No. 39312

- 8 JUL 2019

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IC & SR, I.I.T. MADRAS
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