INDIAN INSTITUTE OF TECHNOLOGY MADRAS
Chennai 600 036

Telephone: [044] 2257 9798/9760 FAX: [044] 22570545/8366
E-mail: arpp@iitm.ac.in

Ref: ELE/RADA/013/2019

Senior Manager (Project Purchase) Date: 25.05.2019

Open Tender No: ELE/RADA/013/2019

Due Date: 19. 06. 2019, 3pm

Pre-Bid meeting: - Not required.

Technical Bid opening meeting on 19. 06. 2019, 4 PM at Department of Electrical Engineering, IIT-Madras.

Dear Sir/Madam,

On behalf of the IIT Madras and CEWiT, offers are invited for the supply of multiple quantities of "**Custom 5GNR FPGA+RF boards**" conforming to the specifications given in Annexure I.

Table 1: Quantity

Item	Quantity CEWIT	Quantity IITM
Custom 5GNR FPGA+RF boards	5	5

Instructions to the Bidder

I. **Preparation of Bids:** - The tenders should be submitted under two-bid system, i.e., Technical bid and Financial bid.

II. **Delivery of the tender:** - The tender shall be sent to the addresses mentioned below, either by post or by courier so as to reach our office before the due date and time specified in our schedule. The offer/bid can also be dropped in the tender box on or before the due date and time specified in the schedule.
The tender box is kept in the office of the:

Senior Manager,
Project Purchase,
IC & SR Building 2nd floor,
I.I.T. Madras,
Chennai – 600 036.
Ph: 044-2257-9798/9723

III. **Opening of the tender:** - The offer/bids will be opened by a committee duly constituted for this purpose. The technical bids will be opened first and will be examined by a technical committee which will decide the suitability of the bids as per our specifications and requirements. All bidders will be invited for opening of technical bids. With respect to opening the financial bid, only technically qualified bidders will be called.

IV. **Prices:** - The price should be quoted in net per unit (after breakup) and must include all packing and delivery charges to **Department of Electrical Engineering.** The offer/bid should be exclusive of taxes and duties. The percentage of tax & duties should be clearly indicated separately. IIT Madras and CEWiT are eligible for concessional GST and relevant certificate will be issued, if applicable.

The price should be quoted without custom duty and GST, since IIT and CEWiT are eligible for concessional GST and customs duty. The price should be quoted on EX-WORKS and CIP basis indicating the mode of shipment.

V. **Agency Commission**: - Agency commission, if any, will be paid to the Indian agents in rupees after receipt of the equipment and its satisfactory installation. Agency Commission will not be paid in foreign currency under any circumstances. The details should be explicitly shown in the tender document even in the case of 'Nil' commission. The tenderer should indicate the percentage of agency commission to be paid to the Indian agent. The foreign Principal should indicate the percentage of payment and it should be included in the basic price quoted originally (if any).

VI. **Terms of Delivery**: - The item(s) should be delivered to the respective institutes based on the purchase order(s). In case of import supply, the item should be delivered at the cost of the supplier to our Institution. The Installation/Commissioning should be completed as specified in our important conditions.

VII. **Technical Bid Opening:** The technical bid will be opened on **19.06. 2019** at 4 p.m. at the **Department of Electrical Engineering, IIT-Madras** and the financial bids of those tenders who are technically qualified will be opened on the same/later date under intimation to them.

VIII. The participating institutes reserve the full right to accept / reject the tender at any stage without assigning any reason.

i) The participating institutes also reserve the right to purchase none or only a subset of the items (as shown in Table 1) without assigning any reason.

ii) The actual quantities ordered may differ based on the requirement at the placement of order.

Yours sincerely,

Senior Manager (Project Purchase)
IC&SR Building, I.I.T. Madras,
Chennai – 600 036.

SCHEDULE

Important Conditions of the tender

1. The due date for the submission of the tender is **19. 06. 2019, 3 pm.**

   The offers / bids should be submitted in two bids systems (i.e.) Technical bid and financial bid. The Technical bid should consist of all technical details / specifications only. The Financial bid should indicate item-wise price for each item and it should contain all Commercial Terms and Conditions including Taxes, transportation, packing & forwarding, installation, guarantee, payment terms, pricing terms etc. The Technical bid and financial bid should be put in separate covers and sealed. Both the sealed covers should be put in a bigger cover. The Open Tender for supply of **"Custom 5GNR FPGA+RF boards"** should be written on the left side of the Outer bigger cover and sealed.

2. **EMD: -** The **EMD in the form of account payee DD for 400,000 Rs in favor of "Registrar IIT Madras" should be enclosed in the cover containing Technical bid.** Any offer not accompanied with the EMD shall be rejected summarily as non-responsive.

   The EMD of the unsuccessful bidders shall be returned within 30 days of the end of the bid validity period. The same shall be forfeited, if the tenderers withdraw their offer after the opening during the bid validity period. The Institute shall not be liable for payment of any interest on EMD. EMD is exempted for Micro and Small Enterprises (MSE) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME).

   When no local agent, the foreign vendor can submit demand draft equal to Rs 400,000 or wire transfer the amount to our account as detailed in the attachment (Annexure II) and enclose the proof with the technical bid.

3. **Performance Security: -** The successful bidder should submit Performance Security for an amount of 5% of the value of the contract/supply. The Performance Security may be furnished in the form of an Account Payee DD, FD Receipt from the commercial bank, Bank Guarantee from any nationalized bank in India. **The performance security should be furnished within 21 days from the delivery of the purchase order.**

   Performance Security in the form of Bank Guarantee:- Incase the successful bidder wishes to submit Performance Security in the form of Bank Guarantee, the Bank Guarantee should be routed through the Beneficiary Bank to the end user bank. Otherwise, the Indian Agent of the foreign vendor has to submit a Bank Guarantee from a Nationalized Bank of India.
   The Bank Guarantee should remain valid for a period of sixty days beyond the date of completion of all contractual obligations of the supplier including the warranty obligations.

4. **Indian agent:** If an Indian agent is involved, the following documents must be enclosed:
   Foreign principal's proforma invoice indicating the commission payable to the Indian Agent and nature of after-sales service to be rendered by the Indian Agent.
   - ✓ Copy of the agency agreement with the foreign principal and the precise relationship between them and their mutual interest in the business.

5. Documentary proof: Please provide data sheets/online links to verify the technical specifications. Please indicate the pages on those documents that refer to specific claims in the technical bid.

6. **Validity:** Validity of Quotation not less than 90 days from the due date of tender.

7. **Delivery Schedule**: - The tenderer should indicate clearly the time required for delivery of the item. In case there is any deviation in the delivery schedule, liquidated damages clause will be enforced or penalty for the delayed supply period will be levied.
   The delivery should be in as per the timeline specified in Annexure 1. If there is delay, the penalty will be @1% per week of delay subject to a max of 10% of the value of purchase order and if the delay is more than 10 weeks, the PO would be cancelled, and liquidated damages will be enforced.

8. **Risk Purchase Clause**:- In the event of failure of supply of the item/equipment within the stipulated delivery schedule, the purchaser has all the right to purchase the item/equipment from other sources on the total risk of the supplier under risk purchase clause.

9. **Advance Payment:** No advance payment is generally admissible. The payment terms are provided in Annexure1. In case of specific percentage of advance payment is required, the Foreign Vendor has to submit a Bank Guarantee equal to the amount of advance payment and it should be routed through the Beneficiary Bank to the end user Bank. Otherwise, the Indian Agent of the foreign vendor has to submit a Bank Guarantee through a Nationalized Bank of India.

10. **On-site Installation**: - The equipment or machinery has to be installed and commissioned by the successful bidder within 20 days from the date of receipt of the item at site of IIT Madras (as applicable).

11. **Late offer**: - The offers received after the due date and time will not be considered. The Institute shall not be responsible for the late receipt of Tender on account of Postal, Courier or any other delay.

12. **Acceptance and Rejection**: - I.I.T. Madras has the right to accept the whole or any part of the Tender or portion of the quantity offered or reject it in full without assigning any reason.

13. **Do not quote the optional items or additional items unless otherwise mentioned in the Tender documents / Specifications.**

14. **Disputes and Jurisdiction**:

Settlement of Disputes: Any dispute, controversy or claim arising out of or in connection with this PO including any question regarding its existence, validity, breach or termination, shall in the first instance be attempted to be resolved amicably by both the Parties. If attempts for such amicable resolution fails or no decision is reached within 30 days whichever is earlier, then such disputes shall be settled by arbitration in accordance with the Arbitration and Conciliation Act, 1996. Unless the Parties agree on a sole arbitrator, within 30 days from the receipt of a written request by one Party from the other Party to so agree, the arbitral panel shall comprise of three arbitrators. In that event, the supplier will nominate one arbitrator and the Project Coordinator of IITM shall nominate on arbitrator. The Dean IC&SR will nominate

the Presiding Arbitrator of the arbitral tribunal. The arbitration proceeding shall be carried out in English language. The cost of arbitration and fees of the arbitrator(s) shall be shared equally by the Parties. The seat of arbitration shall be at IC&SR IIT Madras, Chennai.

a. **The Applicable Law:** This Purchase Order shall be construed, Interpreted and governed by the Laws of India, Court at Chennai shall have exclusive jurisdiction subject to the arbitration clause.
b. Any legal disputes arising out of any breach of contact pertaining to this tender shall be settled in the court of competent jurisdiction located within the city of Chennai in Tamil Nadu.

15. All Amendments, time extension, clarifications etc., will be uploaded on the website only and will not be published in newspapers. Bidders should regularly visit the above website to keep themselves updated. No extension in the bid due date/ time shall be considered on account of delay in receipt of any document by mail.

Acknowledgement: - It is hereby acknowledged that the tenderer has gone through all the conditions mentioned above and agrees to abide by them.

SIGNATURE OF TENDERER
ALONG WITH SEAL OF THE
COMPANY WITH DATE

Annexure I

Bidder Technical Eligibility

a. Please indicate prior FPGA boards (Ultrascale/ Ultrascale+/ MPSOC/ RFSOC) that you have designed and fabricated. Vendors without prior experience (of at least 3 prior boards) of similar complexity will be disqualified. Documentary evidence of the same should be provided.
b. Firm should be in existence for at least 5 years
c. Turnover of more than 10 crores for 3 consecutive years
d. Firm should have, e.g., experience in design and fabrication, of wireless products in LTE that have been demonstrated.
e. Should have a track record of developing standards-based waveforms
f. Should have a demonstrable 5G waveform platform
g. Should have experience in RF Firmware, embedded software design and driver development
h. Firm should have prior experience in RF design and should have supplied to government R&D or Defense or PSU organizations
    i. Work with transceiver IC's such as AD9375/ ASFE7600
    ii. Hardware platforms of similar complexity running baseband stacks

The final evaluation will be based on both the evaluation of the technical expertise of the firm and the financial bid with a weightage ratio of 8:2, i.e., 80% weightage to the technical expertise and 20% on the financial bid. The bidder is required to provide case-studies/ proof of the following criteria while submitting the bid.

Technical criterion

	Points (Total 80)
Prior fabrication and assembly of Ultrascale/ Ultrascale+/ MPSOC/RFSOC boards	5
Prior experience in design and manufacturing LTE wireless products	10
Prior experience in standards-based waveform generation	5
Prior experience in RF design for LTE and ability to handle 23 dBm transmit power.	10
Current ability for 5G waveform generation	5
RF Firmware, Embedded software and driver design experience for Xilinx based FPGA's	5
Technical compliance	40

Delivery Schedule

04 months from the time of awarding the project PO.

Payment Terms

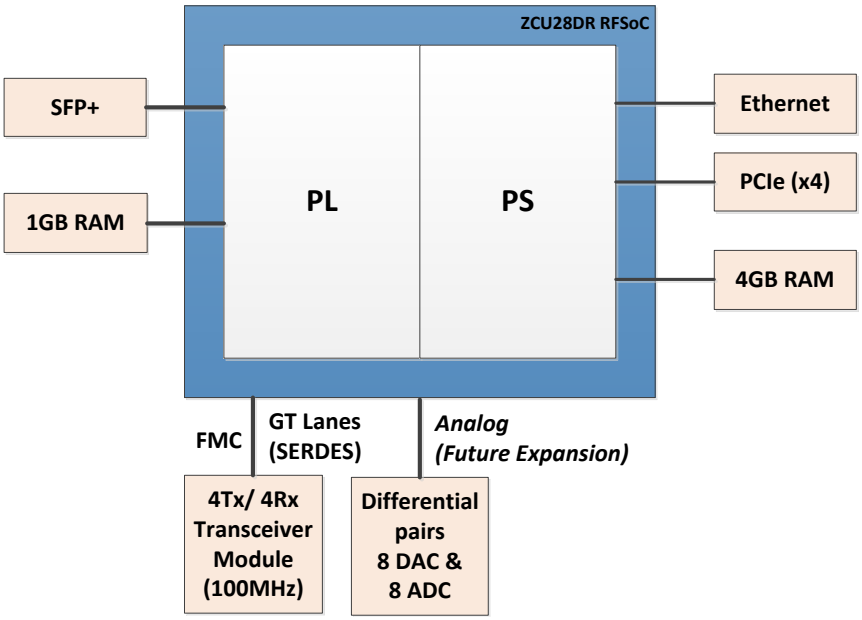
1) 25% at the generation of the Gerber files for fabrication.
2) 25% after the fabrication and assembly of the boards and delivery of one working board.
3) 50% at the delivery of all the units with the required software.

Technical Specifications

We want to procure a total of 10 units (5 units IITM and 5 units CEWiT) of customised FPGA+RF boards that will be used as a 5G NR Hardware and RF transceiver platform. These platforms will be 5G NR proven and delivered with minimal 5G NR waveform demonstrator as described in the specifications below. The GUI Application to be provided will facilitate minimal 5G waveform configurations as specified.

These units should have the following specifications and functions.Digital front end: The digital front end board should consist of a ZCU28DR FPGA, a RFSOC, along with DDR4 memory, micro SD card interface, SFP+ interface (interfaced to the PL) and an ethernet interface to the PS. There should also be an expansion port of PCIe X4 connector. The highspeed transceiver lines and the high sped ADC/DAC lines should terminate in a high speed interface. This high speed interface will be mated with the analog front-end board. The high speed interface should also have enough LVDS lines for the control of the RF front end.

Analog front end: The analog front-end consists of a dual or quad transceiver chip(s) capable of delivering a 4 antenna solution on the platform. The front end should be able to put out 23 dBm power per transmitter and should comply to specifications provided.



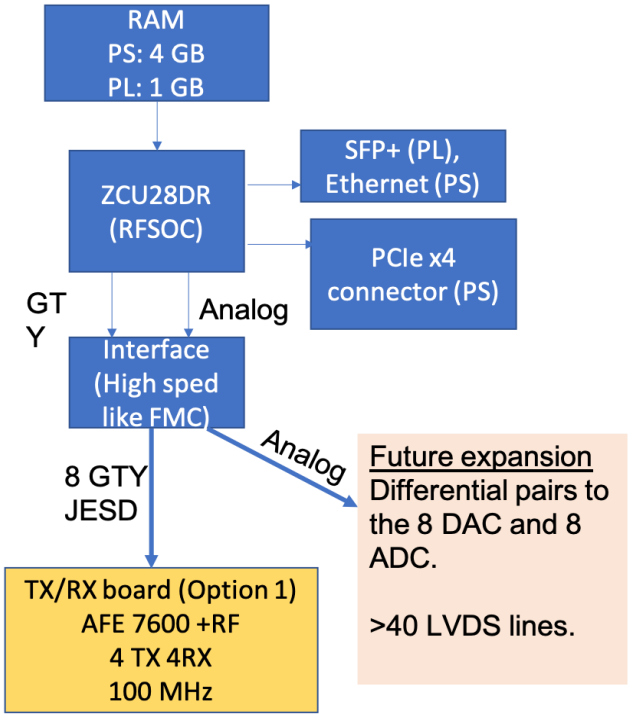


Figure 1: 5G NR System Block diagram. The blue blocks represent the FPGA board (DFE) and the yellow block represents the RF board (AFE). Pink represents the expansion scope

		Remarks
Warranty	6 Months	
Weight	< 1 Kg	
Dimensions (H x W x D)	27 x 17 x 4 cm	
FPGA	ZCU28DR	For prodcution, the FPGA's will be provided by IITMadras.
DDR4 RAM (Processor)	4 GB	
DDR4 RAM (PL)	1 GB	
Interfaces to the Processor		
SD card	1	
Ethernet 1 G	1	
USB (Mini)	1	
UART	1	
PCIe X4 (Mini)	1	
Interfaces to the PL		
10 G SFP+	1	
JTAG	1	

Clocking		
Stable crystal reference	Yes	
GPS option	Yes	Through UART and PPS Input
10 MHZ external reference option	Yes	
High speed connector interfaces		
JESD interfaces	4	
ADC/DAC interfaces	8 ADC, 8 DAC	
LVDS connections	32 pairs	
Power Supply		
Input voltage	12 Volts	
Working temperature	0-55 degrees C	

Analog Front End Specifications

Transceiver Chip	Use JESD based transceiver for Tx and Rx paths	Can be either two dual transceivers or single quad transceiver
# of RF channels	4	
TDD switching	Yes	
Center frequency	3.5 GHz	
Band width	100 MHz	The device shall be capable of atleast 200 MHz
TX power (per channel)	23 dBm	De-embedding of 2dB impedance assumed from Balun + PCB NF + Connectors
ACLR	-35dB or better	
Noise Figure (Without LNA)	- 22dB	Inclusive of connectors/ Baluns
Board NF with LNA	< 3dB	
EVM specifications	0.5% rms	Exact channels and test cases to be used will be defined as part of SoW
Antenna interface	SMA	

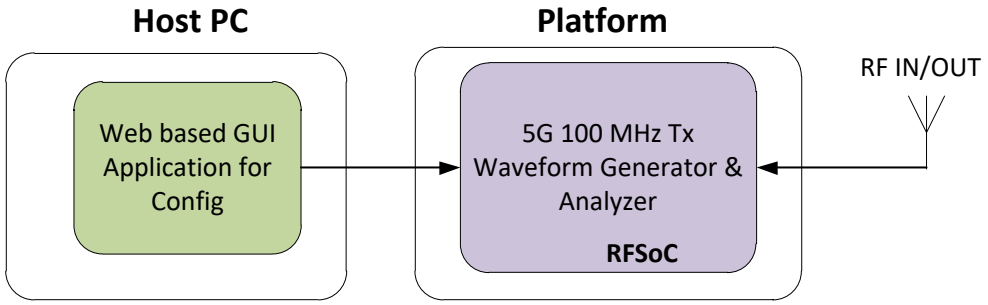
Embedded Software Scope of Work

Slno	Items	Remarks
1	FSBL and U-boot	Xilinx release with customisations
2	Linux 4.xx	Xilinx Release with customisations
3	Device Tree	
4	File System	Xilinx Release with customisations
5	Device Drivers 1. DDR 2. SD CARD 3.QSPI Flash 4. Ethernet – 10/100 10G 5. AXI DMA Drivers -for PS-PL communication 6. UART	

	7. I2C 8. SPI 9. PCIe	

Spcifications of the 5G NR waveform to be demonstrated:

It is required to provide an application that can generate and Transmit 5G waveforms.



Tx Waveform Generator Specifications:

Sl. No.	Parameter	Specification
1	3GPP Standard Specification	Release 15 (FR1)
2	Channels supported	SS Block (PSS,SSS,PBCH) DL Control Channel (PDCCH) DL Shared Channel (PDSCH)
3	Sub Carrier Spacing	15KHz, 30KHz, 60KHz

4	Bandwidth	Upto 100MHz (FR1)
5	Modulation Scheme	QPSK, QAM16, QAM64, QAM256
6	Number of Antenna	1
8	Number of Layers	1

Waveform Analyzer Specifications:

Sl. No.	Parameter	Specification
1	3GPP Standard Specification	Release 15 (FR1)
2	Channels supported	Random Access Channel (PRACH) UL Control Channel (PUCCH) UL Shared Channel (PUSCH)
3	Sub Carrier Spacing	15KHz, 30KHz, 60KHz
4	Bandwidth	Upto 100MHz (FR1)
5	Modulation Scheme	QPSK, QAM16, QAM64, QAM256
6	Number of gNB Antenna	1
8	Number of Layers	1
9	Duplexing Mode	FDD

GUI Application Specifications:

The following configurations will be possible from the GUI Application:

- Config Tool should be Web based Graphical User Interface (GUI).
- It should have options to configure the System parameters like Bandwidth, Numerology, Centre Frequency etc.
- It should be able to set all the downlink and uplink channel configurations.
- It should be able to configure the frame allocations.
- It should have an option to view the allocated frame in a pictorial view.

List of Deliverables:

Schematics		
Bill of Materials		
Layout files		
Gerbers		
FPGA Driver code		
Application Binary for 5G NR demonstrator program		
RFSoC Digital Front end Board	10 NOS	
AFE Transceiver Board	10 NOS	
Embedded Deliverables	FSBL and U-boot	
	Linux 4.xx	
	Device Tree	
	File System	
	Device Drivers 1. DDR 2. SD CARD 3.QSPI Flash	

	4. Ethernet – 10/100 10G 5. AXI DMA Drivers -for PS-PL communication 6. UART 7. I2C 8. SPI 9. PCIe	

Other Details:

1. A detailed architecture and scope of work will be worked out with the selected vendor
2. RFSoC devices will be provided to the selected vendor for use in the project
3. Mechanical design is not a part of the scope of work. However, certain considerations to be incorporated as part of hardware design will be discussed with the selected vendor
4. **Warranty of 06 months to be provided**

Annexure II

CENTRE FOR INDUSTRIAL CONSULTANCY & SPONSORED RESEARCH (IC&SR)
INDIAN INSTITUTE OF TECHNOLOGY MADRAS
CHENNAI 600 036

B NAGARAJAN
JOINT REGISTRAR (IC & SR)

Project Accounts
July 22, 2016

TO WHOMSOEVER IT MAY CONCERN

In connection with project, **US currency may be transferred to CANARA BANK, IIT - MADRAS Branch** with the following details.

FOR TRANSFER OF CURRENCY US DOLLAR

Please Credit in USD **(THROUGH)**

JP MORGAN CHASE, NEW YORK
SWIFT CODE: CHASUS33

For Credit to

USD ACCOUNT No: 001-1395969, of CANARA BANK INTERNATIONAL DIVISION MUMBAI

For Further Credit to

ACCOUNT NO: **2722101001741 of IIT Chennai – Swift Code: CNRBINBBIIT OF THE REGISTRAR, IIT, MADRAS**

JOINT REGISTRAR (IC & SR) i/c
संयुक्त कुलसचिव (आई.सी. एवं एस.आर.)
JOINT REGISTRAR (IC & SR)
आई.आई.टी. मद्रास
I.I.T. MADRAS

This is to certify that the particulars furnished are correct.

For Canara Bank

Senior Manager
Canara Bank - IIT Madras branch

Senior Manager
Canara Bank - Chennai - 36

एस.अरविंदन
S.ARAVINDAN
वरिष्ठ प्रबंधक Senior Manager
S.P.No.31649

Phone : +91 (0) 44 2257 8062 / 8061 / 8060 Fax : +91 (0) 44 2257 0545 / 2257 8366 email : deanicsr@iitm.ac.in website : http://www.iitm.ac.in