INDIAN INSTITUTE OF TECHNOLOGY MADRAS
Chennai 600 036

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V. Sathyanarayanan
Senior Manager (Project Purchase)

Ref: ELE/RADA/003/2019
Date: 25.1.2019

Open Tender No: ELE/RADA/003/2019

Due Date: 15.02. 2019, 3 PM

Pre-Bid meeting: - Not required.

Bid opening meeting on 15.02. 2019, 4 PM at Department of Electrical Engineering, IIT-Madras.

Dear Sir/Madam,

On behalf of the Indian Institute of Technology Madras, offers are invited for **"Xilinx IP Cores"** conforming to the specifications given in Annexure I.

Vendor who can fabricate multilayer Rogers and assemble the board need to respond to the tender please.

Instructions to the Bidder

I. **Preparation of Bids:** - The tenders should be submitted under two-bid system (i.e.) Technical bid and Financial bid.

II. **Delivery of the tender:** - The tender shall be sent to the addresses mentioned below, either by post or by courier so as to reach our office before the due date and time specified in our schedule. The offer/bid can also be dropped in the tender box on or before the due date and time specified in the schedule.
The tender box is kept in the office of the:

Senior Manager,
Project Purchase,
IC & SR Building 2nd floor,
I.I.T. Madras,
Chennai – 600 036.

III. **Opening of the tender:** - The offer/bids will be opened by a committee duly constituted for this purpose. The technical bids will be opened first and will be examined by a technical committee which will decide the suitability of the bids as per our specifications and requirements. All bidders will be invited for opening of technical bids. With respect to opening the financial bid, only technically qualified bidders will be called.

IV. **Prices:** - The price should be quoted in net per unit (after breakup) and must include all packing and delivery charges to **Department of Electrical Engineering.** The offer/bid should be exclusive of taxes and duties. The percentage of tax & duties should be clearly indicated separately. IIT Madras is eligible for concessional GST and relevant certificate will be issued, if applicable.

In case of import supply, the price should be quoted without custom duty. IIT Madras is exempted from levy of IGST on Imports and eligible for concessional custom duty (not exceeding 5%) and the price should be quoted on EX-WORKS and CIP basis indicating the mode of shipment.

V. **Agency Commission**: - Agency commission, if any, will be paid to the Indian agents in rupees after receipt of the equipment and its satisfactory installation. Agency Commission will not be paid in foreign currency under any circumstances. The details should be explicitly shown in the tender document even in the case of 'Nil' commission. The tenderer should indicate the percentage of agency commission to be paid to the Indian agent. The foreign Principal should indicate the percentage of payment and it should be included in the basic price quoted originally (if any)..

VI. **Terms of Delivery**: - The item should be supplied to the **Departments of Electrical Engineering, IIT Madras** as per the Purchase Order. In case of import supply, the item should be delivered at the cost of the supplier to our Institution. The Installation/Commissioning should be completed as specified in our important conditions.

VII. **Technical Bid Opening:** The technical bid will be opened on **15.02.2019** at 4 PM at the **Department of Electrical Engineering, IIT-Madras** and the financial bids of those tenders who are technically qualified will be opened on the same/later date under intimation to them.

VIII. **IIT Madras** reserves the full right to accept / reject any tender at any stage without assigning any reason.

Yours sincerely,

V. Sathyanarayanan
Senior Manager (Project Purchase)
IC&SR Building, I.I.T. Madras,
Chennai – 600 036.

SCHEDULE

Important Conditions of the tender

1. The due date for the submission of the tender is **15.02.2019, 3 PM.**
   The offers / bids should be submitted in two bids systems (i.e.) Technical bid and financial bid. The Technical bid should consist of all technical details / specifications only. The Financial bid should indicate item-wise price for each item and it should contain all Commercial Terms and Conditions including Taxes, transportation, packing & forwarding, installation, guarantee, payment terms, pricing terms etc. The Technical bid and financial bid should be put in separate covers and sealed. Both the sealed covers should be put in a bigger cover. The Open Tender for supply of **"Xilinx IP cores"** should be written on the left side of the Outer bigger cover and sealed.

2. **EMD: -** The **EMD in the form of account payee DD for 2% value of the item in favor of Registrar IIT Madras should be enclosed in the cover containing financial bid.** Any offer not accompanied with the EMD shall be rejected summarily as non-responsive.

   The EMD of the unsuccessful bidders shall be returned within 30 days of the end of the bid validity period. The same shall be forfeited, if the tenderers withdraw their offer after the opening during the bid validity period. The Institute shall not be liable for payment of any interest on EMD. EMD is exempted for Micro and Small Enterprises (MSE) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME).

   When no local agent, the foreign vendor can submit demand draft equal to 2% or wire transfer the amount to our account as detailed in the attachment (Annexure II) and enclose the proof with the financial bid.

3. **Performance Security:** - The successful bidder should submit Performance Security for an amount of 5% of the value of the contract/supply. The Performance Security may be furnished in the form of an Account Payee DD, FD Receipt from the commercial bank, Bank Guarantee from any nationalized bank in India. **The performance security should be furnished within 21 days from the delivery of the purchase order.**

   Performance Security in the form of Bank Guarantee:- Incase the successful bidder wishes to submit Performance Security in the form of Bank Guarantee, the Bank Guarantee should be routed through the Beneficiary Bank to the end user bank. Otherwise, the Indian Agent of the foreign vendor has to submit a Bank Guarantee from a Nationalized Bank of India.
   The Bank Guarantee should remain valid for a period of sixty days beyond the date of completion of all contractual obligations of the supplier including the warranty obligations.

4. **Indian agent:** If an Indian agent is involved, the following documents must be enclosed:
   Foreign principal's proforma invoice indicating the commission payable to the Indian Agent and nature of after-sales service to be rendered by the Indian Agent.
   - ✓ Copy of the agency agreement with the foreign principal and the precise relationship between them and their mutual interest in the business.

5. The offer/bids should be sent only for a machine that is available in the market and supplied to a number of customers. A list of customers in India and abroad with details must accompany the quotations. Quotations for a prototype machine will not be accepted.

6. Original catalogue (not any photocopy) as applicable of the quoted model duly signed by the principals must accompany the quotation in the Technical bid. No prices should ever be included in the Technical bid.

7. **Documentary proof :**
   a. Please provide data sheets (or online links) for the IP cores that are provided.
   b. Xilinx certified vendor or Xilinx authorized distributor.

8. **Validity:** Validity of Quotation not less than 90 days from the due date of tender.

9. **Delivery Schedule**: - The tenderer should indicate clearly the time required for delivery of the item. In case there is any deviation in the delivery schedule, liquidated damages clause will be enforced or penalty for the delayed supply period will be levied.
   Normally the delivery should be in 8 weeks from date of PO (or as specified in Annexure 1 whichever is earlier). If there is delay, the penalty will be @1% per week of delay subject to a max of 10% of the value of purchase order and if the delay is more than 10 weeks, the PO would be cancelled and liquidated damages will be enforced.

10. **Risk Purchase Clause**:- In the event of failure of supply of the item/equipment within the stipulated delivery schedule, the purchaser has all the right to purchase the item/equipment from other sources on the total risk of the supplier under risk purchase clause.

11. **Advance Payment:** No advance payment is generally admissible. In case of specific percentage of advance payment is required, the Foreign Vendor has to submit a Bank Guarantee equal to the amount of advance payment and it should be routed through the Beneficiary Bank to the end user Bank. Otherwise, the Indian Agent of the foreign vendor has to submit a Bank Guarantee through a Nationalized Bank of India.

12. **On-site Installation**: - The equipment or machinery has to be installed or commissioned by the successful bidder within 15 to 20 days from the date of receipt of the item at site of IIT Madras (as applicable).

13. **Late offer**: - The offers received after the due date and time will not be considered. The Institute shall not be responsible for the late receipt of Tender on account of Postal, Courier or any other delay.

14. **Acceptance and Rejection**: - I.I.T. Madras has the right to accept the whole or any part of the Tender or portion of the quantity offered or reject it in full without assigning any reason.

15. **Do not quote the optional items or additional items unless otherwise mentioned in the Tender documents / Specifications.**

16. **Disputes and Jurisdiction**:

Settlement of Disputes: Any dispute, controversy or claim arising out of or in connection with this PO including any question regarding its existence, validity, breach or termination, shall in the first instance be attempted to be resolved amicably by both the Parties. If attempts for such amicable resolution fails or no decision is reached within 30 days whichever is earlier, then such disputes shall be settled by arbitration in accordance with the Arbitration and Conciliation Act, 1996. Unless the Parties agree on a sole arbitrator, within 30 days from the receipt of a written request by one Party from the other Party to so agree, the arbitral panel shall comprise of three arbitrators. In that event, the supplier will nominate one arbitrator and the Project Coordinator of IITM shall nominate on arbitrator. The Dean IC&SR will nominate the Presiding Arbitrator of the arbitral tribunal. The arbitration proceeding shall be carried out in English language. The cost of arbitration and fees of the arbitrator(s) shall be shared equally by the Parties. The seat of arbitration shall be at IC&SR IIT Madras, Chennai.

a. **The Applicable Law:** This Purchase Order shall be construed, Interpreted and governed by the Laws of India, Court at Chennai shall have exclusive jurisdiction subject to the arbitration clause.
b. Any legal disputes arising out of any breach of contact pertaining to this tender shall be settled in the court of competent jurisdiction located within the city of Chennai in Tamil Nadu.

20. All Amendments, time extension, clarifications etc., will be uploaded on the website only and will not be published in newspapers. Bidders should regularly visit the above website to keep themselves updated. No extension in the bid due date/ time shall be considered on account of delay in receipt of any document by mail.

Acknowledgement: - It is hereby acknowledged that the tenderer has gone through all the conditions mentioned above and agrees to abide by them.

SIGNATURE OF TENDERER
ALONG WITH SEAL OF THE
COMPANY WITH DATE

Annexure I

Technical Specifications

Summary: IP cores that run on Xilinx MPSOC FPGA's for the following modules. The license should be a site-based license.

1. 10G/25G Ethernet Subsystem
2. JESD204
3. Digital Pre-Distortion
4. Peak Cancellation Crest Factor Reduction
5. Polar Encoder / Decoder
6. CPRI

Common requirements:

1) **The vendor should provide all the above cores. Partial bidding is not allowed.**
2) All these IPCores should work on MPSOC devices.
3) The committee *may* request the vendor to demonstrate the provided IP's on MPSOC evaluation boards.

Detailed specifications are as follows

1) 10G/25G Ethernet Subsystem

IP Core:
Quantity: 1 site license

10G/25G Ethernet solution should provide a 10 Gigabit or 25 Gigabit per second (Gbps) Ethernet Media Access Controller integrated with a PCS/PMA in BASE-R/KR modes or a standalone PCS/PMA in BASE-R/KR modes. The core should be designed to work with the latest UltraScale and UltraScale+ FPGAs.

Salient Features

- Designed to the 25G Ethernet requirements for 10/25 Gb/s operation specified by IEEE 802.3 Clause 49, IEEE 802.3by, and the 25G Ethernet Consortium
- Low latency 64-bit or 32-bit 10G Ethernet MAC and BASE-R IP
- 10G Ethernet MAC (64-bit) standalone
- 10G and 25G switchable for UltraScale Devices
- Allows multiple instantiations up to by 4
- 10G Ethernet MAC/PCS with 802.1CM (802.3br/802.1bu) pre-emption feature for MAC+PCS/PMA 64-bit Base-R
- BASE-R PCS sublayer operating at 10 Gb/s or 25 Gb/s
    - Optional Auto-Negotiation
    - Optional FEC sublayer
- Custom Preamble mode

Resource Utilization on Ultra-ScalePlus for 25G

LUT: < 6500
FFs: <5500

Latency Specifications

Core	Latency (ns)	User Bus Width (bits)	Core Clock Frequency (MHz)
10GE MAC + PCS	115.2	64	156.25
25GE MAC + PCS	46.08	64	390.625
10G PCS	177.32	64	156.25
25G PCS	71.03	64	390.625
10GE MAC + PCS	36.8	32	312.5

2) JESD204

IP Core
Quantity: 1 site license

The JESD204 IP core should support both B and C configurations. For the B configuration, the line rates of up to 12.5 Gbps should be supported. The IP Core can be configured as JESD204B Transmitter for interfacing to DAC device or JESD204B Receiver for interfacing to ADC device.

The JESD204C IP core should implement a JESD204C compatible interface supporting line rates from 1 Gb/s to 32 Gb/s. Each core supports between 1-8 lane configurations and can be combined with other cores to achieve more lanes.

- JESD204B
    - Designed to JEDEC JESD204B specification
    - Supports scrambling and initial lane alignment
    - Supports 1-256 Octets per frame and 1-32 frames per multi-frame
    - Supports 1 to 32 lane configurations
    - Supports line rates up to 12.5 Gbps certified to the JESD204B spec
- JESD204C
    - Designed to JEDEC JESD204C Standard
    - Supports up to eight lanes per core and greater number of lanes using multiple cores
    - Supports 64B66B and 8B10B link layers
    - Supports FEC Encoding (TX) and Decoding (RX) on the 64B66B link layer
    - Supports CRC-12, CMD and FEC meta data modes on the 64B66B link layer
    - Supports subclass 0 and 1 on the 64B66B link layer and Subclass 0, 1 and 2 on the 8B10B link layer
    - Supports Transceiver sharing between TX and RX cores using the JESD204_PHY core
- All Versions
    - Provides Physical and Data link layer functions
    - AXI4-Stream interface for data
    - AXI4-Lite for configuration interface

Resource utilization on Virtex UltraScale+, 8 lane
LUT<4000
FF< 5053

3) Digital Pre-Distortion (DPD)

IP Core
Quantity: 1 site license

- DPD correction of up to 40 dB of ACLR improvement
- Maximum instantaneous bandwidth of 400MHz
- Support for signal dynamics
- TDD support with automatic data selection
- Feedback receiver Quadrature modulator correction
- PA saturation (overdrive) detection
- Signal capture and analysis
- Easy integration and evaluation using the Debug Interface utility

Physical Configuration Parameters

- Selection of phase options for datapath implementation allowing a resource/sample rate trade off
- Selection of one, two, four or eight transmit antennas
- Selection of two filter/capture depth combinations allowing for resource/performance trade off

4) Peak Cancellation Crest Factor Reduction (PC-CFR)

IP Core
Quantity: 1 site license

- Allows the core to build various architectures for Multi-RAT capability with maximum bandwidth support up to 100MHz in SingleRAT and up to 80MHz in Multi-RAT configurations
- Support for dynamic power and frequency variation
- Support for hard clipper final stage (optional)
- Parameterizable selection of clocks/output sample (1 to 12) to enable optimum area to be achieved with various output sample rates

- Parameterizable selection of Cancellation Pulse Generators (CPG's) (1 to 8) to allow optimum performance vs area trade off.
- Parameterizable selection of number of antennas from 1 to 8
- Single netlist supporting multiple iterations and multiple antennas to reduce overall implementation complexity and improve ease of use
- Increased length of Cancellation Pulse to 2047 to support air interfaces up to 100MHz
- Latency control to allow low latency implementations (Repeater applications)
- Matlab simulator for creation of waveform-specific pulse coefficients and automatic generation of Coregen coefficient file
- C-Model Simulation support

5) Polar Encoder / Decoder

IP Core
Quantity: 1 site license

- Polar encode or decode based on 5G NR (38 series) standards
- Throughput(1) up to:
  - 50 MB/s for decoder (N=1024, K=200)
  - 500 MB/s for encoder (N=1024, K=200)
- High bandwidth AXI4-Stream interfaces

6) CPRI

IP Core
Quantity: 1 site license

- Support CPRI Specification v7.0
- Suitable for use in both Radio Equipment, Controllers (RECs) and Radio Equipment (RE), including multi-hop systems
- 7-Series, UltraScale and UltraScale Plus Should be supported
- Automatic speed negotiation
- Configurable as master or slave, master instantiation can be switched to operate as slave via configuration port
- Supports both Ethernet and HDLC Control and Management channels
- Easy-to-use I/Q data interface together with optional modules for UMTS terrestrial radio access - frequency division duplexing (UTRA-FDD) and Evolved UMTS Terrestrial Radio Access (E-UTRA) data mappings
- Supports vendor-specific data transport including support for the passing of control AxC information in global system for mobile communications (GSM) systems
- Core includes the necessary clocking and transceiver logic to enable easy integration into your design
- Synthesizable example design and simple demonstration test bench provided
- Delay measurement capability meets CPRI Requirement 21 per CPRI Specification v7.0
- Reed-Solomon Forward Error Correction (RS-FEC) supported at 8,110.08 Mb/s, 10,137.6 Mb/s, 12,165.12 Mb/s and 24,330.24 Mb/s line rates

Annexure II

CENTRE FOR INDUSTRIAL CONSULTANCY & SPONSORED RESEARCH (IC&SR)
INDIAN INSTITUTE OF TECHNOLOGY MADRAS
CHENNAI 600 036

B NAGARAJAN
JOINT REGISTRAR (IC & SR)

Project Accounts
July 22, 2016

TO WHOMSOEVER IT MAY CONCERN

In connection with project, **US currency may be transferred to CANARA BANK, IIT - MADRAS Branch** with the following details.

FOR TRANSFER OF CURRENCY US DOLLAR

Please Credit in USD **(THROUGH)**

JP MORGAN CHASE, NEW YORK
SWIFT CODE: CHASUS33

For Credit to

USD ACCOUNT No: 001-1395969, of CANARA BANK INTERNATIONAL DIVISION MUMBAI

For Further Credit to

ACCOUNT NO: **2722101001741 of IIT Chennai – Swift Code: CNRBINBBIIT OF THE REGISTRAR, IIT, MADRAS**

JOINT REGISTRAR (IC & SR) i/c
संयुक्त कुलसचिव (आई.सी. एवं एस.आर.)
JOINT REGISTRAR (IC & SR)
आई.आई.टी. मद्रास
IIT, MADRAS

This is to certify that the particulars furnished are correct.

For Canara Bank

Senior Manager
Canara Bank - IIT Madras branch

एस.अरविंदन
S.ARAVINDAN
Senior Manager
C.R.I.S.P.No.31649

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