



**Dept. of Applied Mechanics,  
Indian Institute of Technology Madras  
Chennai - 36**

Dr. Shaikh Faruque Ali  
Assistant Professor  
Department of Applied Mechanics.

**Phone:** +91(0) 44 2257 4054  
**Fax :** +91(0) 44 2257 4052

**Ref. No.: APM/SHAI/2017/ARDB/ENQ1**

**Date: 16.01.2017**

**Tenders are called for purchase of a Realtime controller system with FPGA**

**DUE DATE:  
08.02.2017**

1. Sealed Quotations are invited in duplicate for the various items shown in Enclosed list (Annexure - I).
2. Sealed Quotations are invited as **TWO-BID** system, i.e., **technical bid** and **financial bid**.
3. The Quotations duly sealed and super scribed on the envelope with the reference No. and due date, should be addressed to the undersigned so as to reach him on or before the due date stipulated above.
4. The Quotations should be valid for sixty days from the due date and the period of delivery required, warranty terms etc. should also be clearly indicated. A minimum of one year warranty required.
5. Brochure detailing technical specifications and performance, list of industrial and educational establishments where the items enquired have been supplied must be provided.
6. Compliancy certificate is to be provided indicating conformity to the technical specifications.
7. If the item is under DGS&D Rate contract No. and the price must be mentioned. It may also please be indicated whether the supply can be made direct to us at the Rate contract price (Please note that we are not Direct Demanding Officers). If so please send copy of the RC.
8. Relevant literature pertaining to the items quoted with full specifications (and drawing, if any) should be sent along with the Quotations, wherever applicable. Samples / machine/ equipment if called for should be submitted / demonstrated at free of charges, and collected back at the supplier's expenses.
9. Packing and delivery charges must be clearly indicated.
10. The rate of sales / General Taxes and the percentage of such other taxes legally leviable and intended to be claimed should be distinctly shown along with the price quoted. Where this is not done, no claim for Sales / General Taxes will be admitted at any stage and on any ground whatsoever The taxes leviable should take into consideration that we are entitled to have concessional Sales Tax applicable to non Government Educational Institutions run with no profit motive for which a concession. Sales Tax Certificate will be issued at the time of final settlement of the bill.
11. Goods should be supplied carriage paid and insured.
12. Goods shall not be supplied without an official supply order.
13. Payment: Every attempt will be made to make payment within 30 days from the date of receipt of bill / acceptance of goods, whichever is later.
14. In case of LC. payment, 90% of the payment will be made after completion of the supply. The balance 10% of the payment will be made after satisfactory installation of the software.
15. IIT Madras is exempt from payment of Excise Duty and is eligible for concessional rate of custom duty. Necessary certificate will be issued on demand. IIT Madras will make necessary arrangements for the clearance of imported goods at the Airport/Seaport. Hence the price should not include the above charges.
16. **Acceptance and Rejection:-** I.I.T. Madras has the right to accept the whole or any part of the Tender or portion of the quantity offered or reject it in full without assigning any reason.

Yours faithfully

Dr. Shaikh Faruque Ali  
Department of Applied Mechanics.

## ANNEXURE – I

Ref. No.: **APM/SHAI/2017/ARDB/ENQ1** Date: **16.01.2017** DUE DATE: **08.02.2017**

SL. NO.	DESCRIPTION	QUANTITY																		
1	<p align="center"><b>Realtime controller system with FPGA module</b></p> <p><i>The realtime controller system should have the following specifications</i></p> <table border="1"> <thead> <tr> <th>Feature</th> <th>Specification</th> </tr> </thead> <tbody> <tr> <td>Real time processor</td> <td> <ul style="list-style-type: none"> <li>Freescale QorIQ P5020, dual-core, 2 GHz</li> <li>32 KB L1 data cache per core, 32 KB L1 instruction cache per core, 512 KB L2 cache per core, 2 MB L3 cache total</li> <li>Freescale QorIQ P1011 800 MHz for communication with host PC</li> </ul> </td> </tr> <tr> <td>Memory</td> <td> <ul style="list-style-type: none"> <li>1 GB DRAM</li> <li>128 MB flash memory</li> </ul> </td> </tr> <tr> <td>Interfaces</td> <td> <ul style="list-style-type: none"> <li>Integrated Gigabit Ethernet host interface Ethernet real-time I/O interface</li> <li>USB 2.0 interface for data logging ("flight recorder") and booting applications via USB mass storage device (max. 32 GB supported)</li> <li>2 CAN channels (partial networking supported)</li> <li>2 x UART (RS232/422/485) interface</li> <li>1 x LVDS interface to connect with the Programmable Generic Interface PGII</li> </ul> </td> </tr> <tr> <td>Programmable FPGA</td> <td> <ul style="list-style-type: none"> <li>Xilinx® Kintex®-7 XC7K325T FPGA and its on chip peripherals;</li> <li>CPU clock: 2 GHz</li> </ul> </td> </tr> <tr> <td>Analog input</td> <td> <ul style="list-style-type: none"> <li>8 x 14-bit channels, 10 Msps, differential; functionality: free running mode</li> <li>24 x 16-bit channels, 1 Msps, differential; functionality: single conversion and burst conversion mode with different trigger and interrupt options</li> <li>Input voltage range: ±10V</li> </ul> </td> </tr> <tr> <td>Analog output</td> <td> <ul style="list-style-type: none"> <li>16 x 16-bit channels, 1 Msps, settling time: 1 μs</li> </ul> </td> </tr> <tr> <td>Digital I/O</td> <td> <ul style="list-style-type: none"> <li>48 bidirectional channels, 2.5/3.3/5 V (single-ended); functionality: bit I/O, PWM generation and measurement (10 ns resolution), pulse generation and measurement (10 ns resolution), 4 x SPI Master</li> <li>12 bidirectional channels (RS422/485 type) to connect sensors with differential interfaces.</li> </ul> </td> </tr> <tr> <td>Sensor supply and Physical Connection</td> <td> <ul style="list-style-type: none"> <li>1 x 12 V, max. 3 W/250 mA (fixed)</li> <li>1 x 2 ... 20 V, max. 1 W/200 mA (variable)</li> <li>4 x Sub-D 50 I/O connectors</li> <li>4 x Sub-D 9 I/O connectors</li> <li>2 x Sub-D 50 I/O connectors</li> <li>48 x BNC I/O connectors</li> <li>4 x Sub-D 9 I/O connectors</li> <li>3 x RJ45 for Ethernet (host and I/O)</li> <li>2 x 2 banana connectors for sensor supply</li> <li>Power supply</li> </ul> </td> </tr> </tbody> </table>	Feature	Specification	Real time processor	<ul style="list-style-type: none"> <li>Freescale QorIQ P5020, dual-core, 2 GHz</li> <li>32 KB L1 data cache per core, 32 KB L1 instruction cache per core, 512 KB L2 cache per core, 2 MB L3 cache total</li> <li>Freescale QorIQ P1011 800 MHz for communication with host PC</li> </ul>	Memory	<ul style="list-style-type: none"> <li>1 GB DRAM</li> <li>128 MB flash memory</li> </ul>	Interfaces	<ul style="list-style-type: none"> <li>Integrated Gigabit Ethernet host interface Ethernet real-time I/O interface</li> <li>USB 2.0 interface for data logging ("flight recorder") and booting applications via USB mass storage device (max. 32 GB supported)</li> <li>2 CAN channels (partial networking supported)</li> <li>2 x UART (RS232/422/485) interface</li> <li>1 x LVDS interface to connect with the Programmable Generic Interface PGII</li> </ul>	Programmable FPGA	<ul style="list-style-type: none"> <li>Xilinx® Kintex®-7 XC7K325T FPGA and its on chip peripherals;</li> <li>CPU clock: 2 GHz</li> </ul>	Analog input	<ul style="list-style-type: none"> <li>8 x 14-bit channels, 10 Msps, differential; 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	<p><b>Software</b></p> <p>a. Software suite for the hardware should be provided. The software should include complete package for the hardware to be used</p>																			

Note: The sealed quotation to be sent to

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Room No. MSB 231  
Department of Applied Mechanics,  
IIT Madras, Chennai-600036, Tamil Nadu, India