INDIAN INSTITUTE OF TECHNOLOGY MADRAS
Chennai 600 036

Telephone: [044] 2257 9763
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The Senior Manager (Project Purchase) Date: 14.11.2023

Open Tender Reference No: EE/GANT/053/2023/PCBASSEMBLY

GEM NAR ID: GEM/GARPTS/03112023/ZVVB578HZE17 Due Date/Time: 04.12.2023 @ 3:00 PM

Dear Sir/Madam,

On behalf of the Indian Institute of Technology Madras, Tenders are invited in two bid system from Class-I local suppliers and Class II local suppliers, for the supply of: "**PCBs Manufacturing and Assembly**" Conforming to the specifications given in **Annexure -A.**

Tender Documents may be downloaded from Central Public Procurement Portal https://etenders.gov.in/eprocure/app. Aspiring Bidders who have not enrolled / registered in e-procurement should enroll / register before participating through the website https://etenders.gov.in/eprocure/app. The portal enrolment is free of cost. Bidders are advised to go through instructions provided at **"Help for contractors".** [Special Instructions to the Contractors/Bidders for the e-submission of the bids online through this eProcurement Portal"]

Bidders can access tender documents on the website (For searching in the NIC site, kindly go to Tender Search option and type „IIT". Thereafter, click on "GO" button to view all IIT Madras tenders). Select the appropriate tender and fill them with all relevant information and submit the completed tender document online on the website https://etenders.gov.in/eprocure/app as per the schedule attached.

1)	**Pre-bid Meeting Details**	**:**	NA
2)	**ICSR Vendor Registration**	**:**	**Vendor registration code.** Vendor registration with IC&SR (IITM) is mandatory for bidders to participate in tenders. ** **For Vendor Registration & Guidelines, Please follow the website :** https://icandsr.iitm.ac.in/vendorportal; Helpdesk: vendorhelpdesk@icsrpis.iitm.ac.in

No manual bids will be accepted. All tender documents including Technical and Financial bids should be submitted in the E-procurement portal.

Last date for receipt of tender	**:**	**04.12.2023 @ 3:00 PM**
Date & time of opening of tender	**:**	**05.12.2023 @ 3:00 PM**

3. Instructions to the Bidder:

A)	**Searching for tender documents**	**:**	• There are various search options built in the CPP Portal, to facilitate bidders to search active tenders by several parameters. These parameters could include Tender ID, organization name, location, date, value, etc. There is also an option of advanced search for tenders, wherein the bidders may combine a number of search parameters such as organization name, form of contract, location, date, other keywords etc. to search for a tender published on the CPP Portal. • Once the bidders have selected the tenders they are interested in, they may download the required documents / tender schedules. These tenders can be moved to the respective **"My Tender"** folder. This would enable the CPP Portal to intimate the bidders through SMS / email in case there is any corrigendum issued to the tender document. • The bidder should make a note of the **unique Tender ID** assigned to each tender, in case they want to obtain any clarification / help from the Helpdesk.
B)	**Assistance to bidders**	**:**	• Any queries relating to the tender document and the terms and conditions contained therein should be addressed to the Tender Inviting Authority for a tender or the relevant contact person indicated in the tender. • Any queries relating to the process of online bid submission or queries relating to CPP Portal in general may be directed to the 24x7 CPP Portal Helpdesk. The contact number for the helpdesk is [0120-4200462, 0120-4001002, 0120-4001005]
C)	**Enrollment Process to Bidders**	**:**	**REGISTRATION** • Bidders are required to enroll on the e-Procurement module of the Central Public Procurement Portal URL:https://etenders.gov.in/eprocure/app by clicking on "Online Bidder Enrollment". Enrollment on the CPP Portal is free of charge. • As part of the enrolment process, the bidders will be required to choose a unique username and assign a password for their accounts. • Bidders are advised to register their valid email address and mobile numbers as part of the registration process. These would be used for any communication from the CPP Portal. • Upon enrolment, the bidders will be required to register their valid Digital Signature Certificate (Class II or Class III Certificates with signing key usage) issued by any Certifying Authority recognized by CCA India (e.g. Sify / TCS / nCode / eMudhra etc.) • Only one valid DSC should be registered by a bidder. Please note that the bidders are responsible to ensure that they do not lend their DSCs to others which may lead to misuse. • Bidder then may log in to the site through the secured log-in by entering their user ID / password and the password of the DSC / eToken. • Possession of a Valid Class II/III Digital Signature Certificate (DSC) in the form of smart card/e-token in the company's name is a prerequisite for registration and participating in the bid submission activities

			through https://etenders.gov.in/eprocure/app ● Digital Signature Certificates can be obtained from the authorized certifying agencies, details of which are available in the web site https://etenders.gov.in/eprocure/app under the "Information about DSC".
D)	**Preparation of bids**	**:**	● Bidder should take into account any corrigendum published on the tender document before submitting their bids. ● Please go through the tender advertisement and the tender document carefully to understand the documents required to be submitted as part of the bid. Please note the number of covers in which the bid documents have to be submitted, the number of documents including the names and content of each of the document that need to be submitted. Any deviations from these may lead to rejection of the bid. ● Bidder, in advance, should prepare the bid documents to be submitted as indicated in the tender document / schedule and generally shall be in PDF / XLS formats as the case may be. Bid documents may be scanned with 100 dpi with black and white option. ● To avoid the time and effort required in uploading the same set of standard documents which are required to be submitted as a part of every bid, a provision of uploading such standard documents (e.g. PAN card copy, GSTIN Details, annual reports, auditor certificates etc.) has been provided to the bidders. Bidders can use **"My Documents"** area available to them to upload such documents. These documents may be directly submitted from the **"My Documents"** area while submitting a bid, and need not be uploaded again and again. This will lead to a reduction in the time required for bid submission process.
E)	**Submission of bids**	**:**	● Bidder should log into the site well in advance for bid submission so that he/she can upload the bid in time i.e. on or before the bid submission date and time. Bidder will be responsible for any delay due to other issues. ● The bidder has to digitally sign and upload the required bid documents one by one as indicated in the tender document. ● Bidder has to select the bid security declaration. Otherwise, the tender will be summarily rejected. ● A standard BOQ format has been provided with the tender document to be filled by all the bidders. Bidders are requested to note that they should necessarily submit their financial bids in the format provided and no other format is acceptable. Bidders are required to download the BOQ file, open it and complete the detail with their respective financial quotes and other details (such as name of the bidder). If the BOQ file is found to be modified by the bidder, the bid will be rejected. ● The server time (which is displayed on the bidders" dashboard) will be considered as the standard time for referencing the deadlines for submission of the bids by the bidders, opening of bids etc. The bidders should follow this time during bid submission. ● The Tender Inviting Authority (TIA) will not be held responsible for any sort of delay or the difficulties faced during the submission of bids online by the bidders due to local issues. ● The uploaded tender documents become readable only after the tender opening by the authorized bid openers.

			● Upon the successful and timely submission of bids, the portal will give a successful bid submission message & a bid summary will be displayed with the bid no. and the date & time of submission of the bid with all other relevant details. ● Kindly add scanned PDF of all relevant documents in a single PDF file of compliance sheet. ● More information useful for submitting online bids on the CPP Portal may be obtained at: https://etenders.gov.in/eprocure/app. ● All tender documents including pre-qualification bid, Technical Bid &Financial Bid should be submitted separately in online CPP portal as per the specified format only. Right is reserved to ignore any tender which fails to comply with the above instructions. **No manual bid submission will be entertained.**
F)	**Marking on Technical Bid**		● The bidder eligibility criteria, technical specification and supply of item for this tender is given in Annexure B. ● The Bidders shall go through the specification and submit the technical bid. ● The Technical bid should be submitted in the proforma as per Annexure-B in pdf format only through online (e-tender). No manual submission of bid will be entertained. ● The technical bid should have a page-wise heading as "Technical Bid" and page no. in all pages with seal and signature of authorized signatory. The total no. of pages should be mentioned at the last page of the documents. ● The technical bid should consist of bidder eligibility criteria details and all technical details along with catalogue/ pamphlet which will give a detailed description of product with technical data sheet so that technical compliance can be verified.
G)	**Marking on Price Bid**		● Financial bid (BoQ) should be submitted in the prescribed proforma format as per Annexure-C in xls format through e-tender only. No manual or other form of submission of Financial Bid will not be entertained

4)	**Preparation of Tender:** The bidders should submit the bids in two bid system as detailed below. **Bid I _Technical Bid** The technical bid should consist of bidder eligibility criteria and technical specification compliance sheet as per Annexure-B. **Bid II _Price Bid** The price bid should be submitted in excel format (BoO) as per the proforma (Annexure C) uploaded in the e-Tender web site. The Quoted price should be for supply and installation of the item and inclusive of all cost and statutory levies at IIT Madras.
5)	**Price:** a) The price should be quoted only in INR net per unit (after breakup) and must include all packing, transit insurance and delivery charges to the **Department of Electrical Engineering**. b) The rate quoted shall be all inclusive of all taxes and no extra payment will be made other than statutory revisions as per the terms and conditions stipulated in this contract document c) The percentage of tax & duties should be clearly indicated separately. IIT Madras is eligible for custom duty (5.5%). Relevant certificates will be issued wherever necessary d) The offer/bids should be submitted through online only in two bid system i.e. Technical Bid and Financial Bid separately.
6)	**Tenderer shall submit along with this tender:** (i) Proof of having ISO or other equivalent certification given by appropriate authorities. (ii) Name and full address of the Banker and their swift code and PAN No. and GSTIN number. (iii) GST registration proof showing registration number, area of registration etc. (iv) All of your future correspondences including Invoices should bear the GST No. and Area Code.
7)	**Terms of Delivery:** Supplier will be fully responsible for the safe carriage, Installation/Commissioning of goods up to the **Department of Electrical Engineering**, IIT Madras or named place as per PO, Insurance coverage will be in the scope of the supplier. The tenderer should indicate clearly the time required for delivery of the item (subject to the approval of the Executive Committee-IIT-Madras). In case there is any deviation in the delivery schedule, liquidated damages clause will be enforced or penalty for the delayed supply period will be levied. In the event of delay or non-supply of materials/execution of Contract beyond the date of delivery/completion of job. The penalty will be levied @1% per week of delay subject to a max of 10% of the value of purchase order and if the delay is more than accepted time frame by IIT M, the PO would be partially or fully cancelled and liquidated damages will be enforced accordingly.
8)	**Period for which the offer will remain open:** The Tender shall remain open for acceptance/validity till: 120 days from the date of opening of the tender. However, the day up to which the offer is to remain open being declared closed holiday for the Indian Institute of Technology Madras, the offer shall remain open for acceptance till the next working day.

9)	**EMD:** The EMD of Rs. 1,40,000 to be transferred to the account details mentioned in Annexure D and proof should be enclosed in the Technical Bid. Any offer not accompanied with the EMD shall be rejected summarily as non-responsive. The EMD of the unsuccessful bidders shall be returned within 30 days of the end of the bid validity period. The same shall be forfeited, if the tenderers withdraw their offer after the opening during the bid validity period. The Institute shall not be liable for payment of any interest on EMD. EMD is exempted for Micro and Small Enterprises (MSE) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME) and Startups as recognized by Department of Industrial Policy & Promotion (DIPP). (MSE/MSME/DIPP PROOF should be enclosed in the cover containing technical bid).
10)	**Performance Security: -** **The successful bidder should submit Performance Security for an amount of 5% of the value of the contract/supply**. The Performance Security may be furnished in the form of an Account Payee DD, FD Receipt in the name of "The Registrar, IIT Madras" from any scheduled commercial bank or Bank Guarantee from any scheduled commercial bank in India. The performance security should be furnished within 14 days from the date of the purchase order. Performance Security in the form of Bank Guarantee: - In case the successful bidder wishes to submit Performance Security in the form of Bank Guarantee, the Bank Guarantee should be routed directly to IIT Madras from the Bank. The Bank Guarantee should remain valid for a period of sixty days beyond the date of completion of all contractual obligations of the supplier including the warranty obligations.
11)	For the same tender, either the OEM or the authorized dealer/service provider can only quote. But bothof them cannot quote separately for the same tender.
12)	The offers/bids should be sent only for a item/Equipments of latest version that is available in the market and supplied to a number of customers. A list of customers in India with details must accompany the quotations. Quotations for a prototype machine will not be accepted
13)	Original catalogue (not any photocopy) of the quoted model duly signed by the principals must accompany the quotation in the Technical bid.
14)	Compliance or Confirmation report with reference to the specifications and other terms & conditions should also be obtained from the principal/OEM.
15)	**Risk Purchase Clause** In the event of failure of supply of the item/equipment within the stipulated delivery schedule, the purchaser has all the right to purchase the item/equipment from other sources on the total risk of the supplier under risk purchase clause.
16)	**Payment:** i. Two-stage **payment** a. **Stage 1:** 40% Payment will be done once stage 1 is completed and is delivered. b. **Stage 2**: 60% Payment will be done once stage 2 is completed and is delivered. (ii) Advance Payment: No advance payment is generally admissible. In case a specific percentage of advance payment is required, the Vendor has to submit a Bank Guarantee from a scheduled commercial bank in India equivalent to the amount of advance payment.
17)	**On-site Installation:** The equipment/item or Machinery has to be installed or commissioned by the successful bidder within the number of days (as prescribed by PI) from the date of receipt of the item at the site of IIT Madras.

18)	**Warranty/Guarantee:** The offer should clearly specify the warranty or guarantee period for the machinery/equipment. Any extended warranty offered for the same has to be mentioned separately (For more details please refer our Technical Specifications). **** Note: PO which involves installation, warranty/guarantee shall be applicable from date of installation.**
19)	**Acceptance and Rejection:** Failure to comply with any of the instructions stated in this document or offering unsatisfactory explanations for non-compliance will likely to lead to rejection of offers. I.I.T. Madras has the right to accept the whole or any part of the Tender or portion of the quantity offered or reject it in full without assigning any reason.
20)	**Debarment from Bidding:** In case of breach of Terms & Conditions, Bidder may be suspended from being eligible for bidding in any contract with the IIT Madras up to 2 Years [as per Rule 151(iii) of GFR] from the date of Tender.
21)	**Disputes and Jurisdiction:** **Settlement of Disputes:** Any dispute, controversy or claim arising out of or in connection with this PO including any question regarding its existence, validity, breach or termination, shall in the first instance be attempted to be resolved amicably by both the Parties. If attempts for such amicable resolution fails or no decision is reached within 30 days whichever is earlier, then such disputes shall be settled by arbitration in accordance with the Arbitration and Conciliation Act, 1996. Unless the Parties agree on a sole arbitrator, within 30 days from the receipt of a written request by one Party from the other Party to so agree, the arbitral panel shall comprise of three arbitrators. In that event, the supplier will nominate one arbitrator and the Project Coordinator of IITM shall nominate on arbitrator. The Dean IC&SR will nominate the Presiding Arbitrator of the arbitral tribunal. The arbitration proceeding shall be carried out in English language. The cost of arbitration and fees of the arbitrator(s) shall be shared equally by the Parties. The seat of arbitration shall be at IC&SR IIT Madras, Chennai. a. The Applicable Law: The Purchase Order shall be construed, interpreted and governed by the Laws of India. Court at Chennai shall have exclusive jurisdiction subject to the arbitration clause. b. Any legal disputes arising out of any breach of contact pertaining to this tender shall be settled in the court of competent jurisdiction located within the city of Chennai in Tamil Nadu.
22)	**Force Majeure:** The Supplier shall not be liable for forfeiture of its performance security, liquidated damages or termination for default, if and to the extent that, it‟s delay in performance or other failure to perform its obligations under the Contract is the result of an event of Force Majeure. For purposes of this Clause, “Force Majeure” means an event beyond the control of the Supplier and not involving the Supplier’s fault or negligence and not foreseeable. Such events may include, but are not limited to, acts of the Purchaser either in its sovereign or contractual capacity, wars or revolutions, fires, floods, epidemics, quarantine restrictions and freight embargoes. If a Force Majeure situation arises, the Supplier shall promptly notify the Purchaser in writing of such conditions and the cause thereof. Unless otherwise directed by the Purchaser in writing, the Supplier shall continue to perform its obligations under the Contract as far as is reasonably practical, and shall seek all reasonable alternative means for performance not prevented by the Force Majeure event.

23)	**Eligibility Criteria:** **As per the Government of India Order, only "Class - I Local Suppliers" and "Class - II Local Suppliers" can participate in this tender.** **Bidder should confirm their acceptance that they comply with the provisions with report to "Guidelines for eligibility of a bidder from a country which shares a land border with India as detailed at Annexure-F. The bidder should submit Certificate for "Bidder from/ Not from Country sharing Land border with India & Registration of Bidder with Competent Authority" as per Order of DoE F.No.6/18/2019-PPD dated 23.07.2020 as mentioned.**
24)	**Preference to "class I Local Suppliers"**: preference will be given to "**class 1 local suppliers**" (subject to class -I local supplier's quoted price falling within the margin of purchase preference) as per public procurement (preference to make in India) order 2017 .O.M No P- 45021/2/2017 – pp(BE - 11) dt 04/06/2020 subject to the conditions that the "class 1 Local Supplier" should agree to supply goods / provide service at L1 rate and furnish a certificate with the technical bid document that the goods/service provided by them consists local content equal to or more than 50%.(certificate from Chartered Accountant in case value of contract exceeds Rs 10 crore). **"Class - I local supplier"** means a supplier or service provider whose goods, services or works offered for procurement consists of local content equal to or more than 50% as defined under the above said order. **Declaration to be provided as per Annexure-II per item/service/work.** **"Class - II local supplier"** means a supplier or service provider whose goods, services or works offered for procurement consists of local content equal to 20% but less than 50% as defined under the above said order. **Declaration to be provided as per Annexure-II per item/service/work.** **"Margin of purchase preference"**: - The margin of purchase preference shall be 20%. The Definition of the margin of purchase preference is defined in the Govt. of India Order No: **P-45021/12/2017-PP (BE-II) Dt.4th June, 2020) Order 2017. As per the Government of India Order – "Margin of Purchase Preference" means the maximum extent to which the price quoted by a "Class-I local supplier" may be above the L1 for the purpose of purchase preference.** ****Note: Local content percentage to be calculated in accordance with the definition provided at clause 2 of revised public procurement preference to Make in India Policy vide GoI Order no. P-45021/2/2017-PP (B.E.-II) dated 15.06.2017 (subsequently revised vide orders dated 28.05.2018, 29.05.2019and 04.06.2020) MOCI order No. 45021/2/2017-PP (BE II) Dt.16th September 2020 & P-45021/102/2019-BE-II-Part(1) (E-50310) Dt.4th March 2021**

25)	**Evaluation of Bids** Bid evaluation will take place in two stages. **Stage I Technical Bid evaluation** All bidders who have fully complied with bidder eligibility criteria I, II and technical evaluation (Annexure B) will only be considered for opening of price bid. **Stage II: Price Bid Evaluation** The price bid evaluation will be based on price quoted by the bidder. The rate quoted for **PCBs Manufacturing and Assembly** unit will alone be taken up for arrival of Lowest Bid (L1) value.
26)	In accordance to the Rule 173 of GFR,2017 and relevant provisions thereof in Procurement Manuals, 2022,IC&SR, IITM reserves the right to carry out the negotiation process through its purchase/technical committee with L1/H1 (as applicable) vendor to ensure price reasonability before final recommendation to the Competent Authority. The negotiation details, if any, on case to case basis shall be recorded in minutes of meetings suitably for records.
27)	**Selection of successful bidder and Award of Order** The order will be directly awarded to the technically qualified bidder as per the condition in para 3A of DIPP, MoCI Order No. 45021/2/2017-PP (BE II) dated 16th September 2020.
28)	All information including selection and rejection of technical or financial bids of the prospective bidders will be communicated through e-Tender portal. In terms of Rule 173(iv) of General Financial Rule 2017, the bidder shall be at liberty to question the bidding conditions, bidding process and/or rejection of bids.
29)	The tenderer shall certify that the tender document submitted by him / her are of the same replica of the tender document as published by IIT Madras and no corrections, additions and alterations made to the same. If any deviation found in the same at any stage and date, the bid / contract will be rejected / terminated and actions will be initiated as per the terms and conditions of the contract.
30)	Clarification to the queries and doubts raised by the bidders will be issued as a corrigendum/addendum in the e-tenders portal.
31)	In the e-tender process, participation of bidders after the due date is not possible. The eligible bidders can login to the e-Procurement portal to ascertain the tender status.

ACKNOWLEDGEMENT

It is hereby acknowledged that I/We have gone through all the points listed under "Specification, Guidelines, Terms and Conditions" of tender document. I/We totally understand the terms and conditions and agree to abide by the same.

SIGNATURE OF TENDERER ALONG
WITH SEAL OF THE COMPANY WITH DATE

ANNEXURE – A

Bidder Eligibility Criteria and Technical Specification for PCBs Manufacturing and Assembly
Tender No. EE/GANT/053/2023/PCBASSEMBLY

Bidder Eligibility Criteria – I (Public Procurement – Preference to Make in India)

Only 'Class-I local suppliers' and 'Class-II local suppliers', as defined under DIPP, MoCI Order No. P-45021/2/2017-PP (BE-II) dated 16th September 2020 and other subsequent orders issued therein.

CHECKLIST

Please ensure that the following compliance sheets are in your technical bid

Particulars
Compliance sheet: 1
Compliance sheet: 2
Compliance sheet: 3
Compliance sheet: SOM
Compliance sheet: Integrated Mother Board
Compliance sheet: SOM EVK Mother Board

The technical details for PCB and assembly are provided below. The BOM for the boards will be providedas Excel sheet upon request. Please email rganti@ee.iitm.ac.in and subashini@5gtbiitm.in

Bidder Eligibility Criteria – II

1. The Firm should have a minimum turnover of 5 crores/year.Evidence should be provided.
2. The vendor must provide proof of business with other clients (atleast 2) in the past year and can provide client references.
3. The Firm should be in business for a minimum of 5 years.Evidence should be provided.
4. Please indicate prior High-Speed FPGA and high-power RF boards (of similar complexity of at least 12 layers) that you have fabricated. Vendors without prior experience (of at least two prior boards) of similar complexity will be disqualified. Documentary evidence of the same should be provided.
5. Explicitly indicate the PCB Fab details for each board and **its technical capabilities**, where each board will be fabricated. References to online material/documentation for verification **should** be provided. The bid might be disqualified if the technical capabilities of the proposed FAB are not clear or do notmeet the technical requirements of the boards.

    1) The country of the FAB should explicitly be mentioned.
        a. If these boards are manufactured in countries that sharea land border with India, the bid will be eligible only if the FAB is registered with the competent authority and the required approvals are obtained as mentioned in the GFR amendments (Rule 144 (xi)) posted on 23rd July 2020.
        b. These required approvals have to be part of the technicaltender for the bid to be valid.

6. Prior engineering compliance with the FAB (for meeting the technical specifications, as mentioned in the subsequent sections) for manufacturing the required PCB should be provided (for each PCB) in the templates provided in the next sections.

1. The confirmation from the FAB (as email exchange or letters (in English)) should also be provided in the tender.

2. Some important considerations

- Most of the boards require blind vias.
- Impedance control is required

7. Explicitly indicate the plant details **and its technical capabilities**, where the board will be assembled.

8. Please indicate the country of the assembly facility. **The assembly facility should be in India**

- Where IITM can ship the required components (FPGA's, ICs, Transceivers)
- The assembly plant and testing facility should be in India and should be ready for rework as the case arises without additional cost
- Support for double-sided PCB assembly

9. Assembly should have the capability of IPC-610 class2 and class 3 standards

10. The assembly line should be capable of handling 01005 discrete components, 0.4 mm BGA's, 0.4 mm pitch, LGA CC-20-3, andshould have the capability of odd angle placement

11. Assembly Should have the facility for flying probe testers and automated optical lines (inspection)

12. Assembly should have in house X-ray inspection should be available.

III. Technical Specification for PCBs Manufacturing and Assembly

1) Technical Specifications, quantities for compliance

The following boards are going to be manufactured. All the boards have two stages of manufacturing.

Stage1: PCB fab and assembly for X no of boards. The exact numbers for assembled and bare boards are provided below.
Stage 2: PCB fab and assembly for Y no of boards. The exact numbers for assembled are provided below.

S. No	Board name	Quantity for Stage 1			Quantity for Stage 2	Total Quantity
		Bare Board	Power & Clock Board	Full Assembly	Full Assembly	
1	SOM	1	1	4	14	20
2	Integrated Mother Board	1	0	2	4	7
3	SOM EVK Mother Board	1	0	2	4	7

*There will be minor design changes between Stage 1 and Stage 2.

Compliance Sheet 1:

S. No	
1	There may be design changes in the PCBs (schematics and layout) between Stage 1 and Stage2. Also a few components (around 5%)might change based on the outcomes of each stage. The Vendor should be able to accommodate these.
2	Open, Short, and Impedance reports must be submitted before and after Assembly to IIT Madras for validation of the quality of Fabrication and Assembly for 1st Stage. (Exact Test points will be shared along with Gerbers)
3	Complete Test Procedure with detailed Steps will be shared for the 2nd Stage, In addition to Open Short and Impedance testing this includes: 1. Power On test 2. Clock Programming 3. Booting
4	IIT Madras only will be paying for boards that have passed the tests and been approved and validated by IITM

Compliance sheet 2:

1. Turnaround time from the receipt of the PO tillthe fabrication and assembly of the boards for Stage 1 **– 8 Wee**ks
2. Turnaround time from the receipt of the go ahead till the fabrication and assembly of the boards for Stage 2 – **8 Weeks**

TERMS AND CONDITIONS

Compliance sheet 3

1. The delivery time cannot be changed

2. All the boards have been quoted. If some boards are not quoted the vendor will be dis-qualified

3. The stack up, PCB pre-peg and Core materials of the boards, the via and Trace dimensions and any technical specifications of these boards were **designed after extensivesimulations and will be impossible to change.**

Attached Stack-up has been verified by the following Fabricators:

1) HiQ
2) Phase-3
3) Micro-pack

We encourage the bidders to Fabricate boards from the above Vendors
for quick turn around time. But, bidders are allowed to Fabricate with any other reputed Vendor(as per the tender clauses) as along as the Stack-up and Timeline remains same

4. Basic rework might be requested (as required) and the vendor should support this without any additional cost

5. PCB fabrication: At the end of Stage1, the firm should provide us with a report on the PCBs that were fabricated and assembled and proceed withthe assembly only after technical approval by the IITM team.

6. In the financial bid, the fabrication cost of each PCB, BOM cost, andAssembly cost are separately and explicitly mentioned.

7. Will provide the BOM as per the requirements for all the boards. The BOMfor the boards will be provided as excel sheet upon request. Please email rganti@ee.iitm.ac.in and subashini@5gtbiitm.in. Part of the BOM for assembly will be provided by IIT-Madras.

8. BOM supplied by the Vendor should have warranty and COC certification

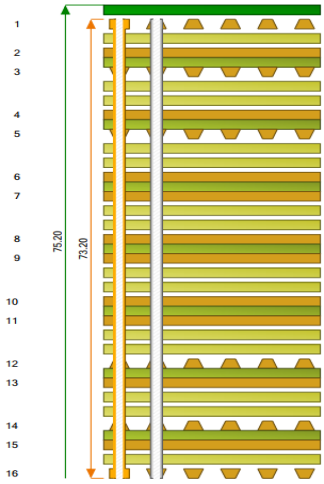
2 BOARD FABRICATION SOM

Compliance Sheet SOM

1. Country where PCB will be manufactured.
2. FAB name where PCB will be manufactured.
3. FAB technical capability details areprovided (As separate sheets)
4. Company where PCB will be Assembled in India

S. No	Description	Specification
A	**PCB FABRICATION**	
1	No. of layers	16
2	Via Technology	Through Hole and Blind Via With back drilling option
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40
4	Impedance control (Yes/No) Mention tolerance	Yes
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: a. Signal Layer Thickness 0.689 mil b. Power (Including ground) layers 0.689 mil and 2.638 mil

7	Min. finished hole dia (mil)	8 Mil Mech
8	Min. trace width (mil)	3
9	Min. spacing (mil)	3
10	Min. Annular ring (mil)	6
11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig
12	PCB Dimension in mm	125 mm X 90 mm +/- 10%
13	Metal core board	No
14	Mil Grade	No
15	Whether Group B Test Report required	No
16	Solder Mask Colour	Green
17	Silkscreen Colour	White
18	RoHS Complaint	Yes
19	UL Logo Required	Yes
20	Back Drilling Required	No
21	RF VIAS	No
B	**STACKUP REQUIREMENTS**	
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper
23	Specify Compliance to the Stack up at the bottom	
24	Specify Compliance to the Impedance table at the bottom	
C	**ASSEMBLY**	
25	No of comps per board	1000
26	No of BGAs per board	10
27	Maximum pin count	1516, 1 mm BGA
28	Minimum BGA pitch	1 mm
29	Total No of points to be soldered (no of Pins)	6000(approx)
30	PTH pins	300
31	Both side assembly	Yes
32	Board Size-	125 mm X 90 mm+/- 10%
33	Board Thickness	75.196 Mils
34	No of Layers	16
35	X-ray verification of all BGA's, LPA and QFN	Yes. Test results should be provided.
36	AOI report for the components	Yes, Report needed
37	Manual Inspection of Q&A for all I. C's	Yes, Report needed

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
3		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
5		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
7		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
9		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
11		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
13		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
15		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

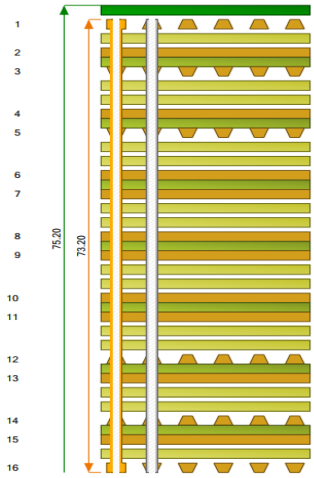
3 BOARD FABRICATION INTEGRATED MOTHER BOARD

Compliance Sheet SOM

1. Country where PCB will bemanufactured
2. FAB name where PCB will bemanufactured.
3. FAB technical capability details areprovided (As separate sheets)
4. Company where PCB will beAssembled in India

S. No	Description	Specification
A	**PCB FABRICATION**	
1	No. of layers	16
2	Via Technology	Through Hole and Blind Via With back drilling option
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40
4	Impedance control (Yes/No) Mention tolerance	Yes
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: c. Signal Layer Thickness 0.689 mil d. Power (Including ground) layers 0.689 mil and 2.638 mil
7	Min. finished hole dia (mil)	8 Mil Mech
8	Min. trace width (mil)	3
9	Min. spacing (mil)	3
10	Min. Annular ring (mil)	6
11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig

12	PCB Dimension in mm	125 mm X 90 mm +/- 10%
13	Metal core board	No
14	Mil Grade	No
15	Whether Group B Test Report required	No
16	Solder Mask Colour	Green
17	Silkscreen Colour	White
18	RoHS Complaint	Yes
19	UL Logo Required	Yes
20	Blind Vias Buried Vias Back Drilling Required	Yes
21	RF VIAS	No
B	**Stackup Requirements**	
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper
23	Specify Compliance to the Stack up at the bottom	
24	Specify Compliance to the Impedance table at the bottom	
C	**Assembly**	
25	No of comps per board	500
26	No of BGAs per board	10
27	Maximum pin count	540, 1 mm LPGA
28	Minimum BGA pitch	0.8 mm
29	Total No of points to be soldered (no of Pins)	6000(approx)
30	PTH pins	300
31	Both side assembly	Yes
32	Board Size-	450 mm X 400 mm+/- 10%
33	Board Thickness	75.196 Mils
34	No of Layers	16
35	X-ray verification of all BGA’s, LPA and QFN	Yes. Test results should be provided.
36	AOI report for the components	Yes, Report needed
37	Manual Inspection of Q&A for all I. C’s	Yes, Report needed



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	er	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
3			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
5			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
7			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
9			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
11			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
13			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
15			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	er	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

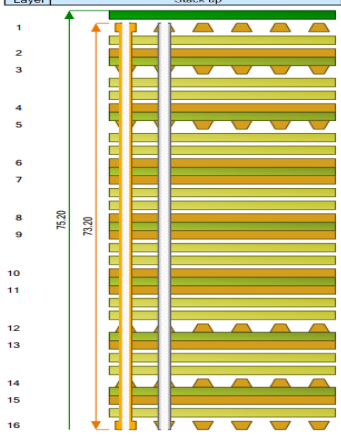
4 BOARD FABRICATION SOM EVK MOTHER BOARD

Compliance Sheet SOM EVK Mother Board

1. Country where PCB will be manufactured.
2. FAB name where PCB will be manufactured.
3. FAB technical capability details areprovided (As separate sheets)
4. Company where PCB will beAssembled in India

S. No	Description	Specification
A	**PCB FABRICATION**	
1	No. of layers	16
2	Via Technology	Through Hole and Blind Via With back drilling option
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40
4	Impedance control (Yes/No) Mention tolerance	Yes
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: e. Signal Layer Thickness 0.689 mil f. Power (Including ground) layers 0.689 mil and 2.638 mil
7	Min. finished hole dia (mil)	8 Mil Mech
8	Min. trace width (mil)	3
9	Min. spacing (mil)	3
10	Min. Annular ring (mil)	6

11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig
12	PCB Dimension in mm	170 mm X 170 mm +/- 10%
13	Metal core board	No
14	Mil Grade	No
15	Whether Group B Test Report required	No
16	Solder Mask Colour	Green
17	Silkscreen Colour	White
18	RoHS Complaint	Yes
19	UL Logo Required	Yes
20	Back Drilling Required	No
21	RF VIAS	No
B	**STACKUP REQUIREMENTS**	
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper
23	Specify Compliance to the Stack up at the bottom	
24	Specify Compliance to the Impedance table at the bottom	
C	**ASSEMBLY**	
25	No of comps per board	500
26	No of BGAs per board	10
27	Maximum pin count	540, 1 mm LPGA
28	Minimum BGA pitch	0.8 mm
29	Total No of points to be soldered (no of Pins)	6000(approx)
30	PTH pins	300
31	Both side assembly	Yes
32	Board Size-	125 mm X 90 mm+/- 10%
33	Board Thickness	75.196 Mils
34	No of Layers	16
35	X-ray verification of all BGA’s, LPA and QFN	Yes. Test results should be provided.
36	AOI report for the components	Yes, Report needed
37	Manual Inspection of Q&A for all I. C’s	Yes, Report needed



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
3			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
5			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
7			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
9			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
11			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
13			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
15			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

TWO STAGE PAYMENT

Stage 1:40% Payment will be done once the stage 1 is completed and is delivered.
Stage 2:60% Payment will be done once the stage 2 is completed and is delivered.

SIGNATURE OF BIDDER ALONG WITH SEAL OF THE COMPANY WITH DATE

ANNEXURE - B

TECHNICAL BID PROFORMA

Tender No. EE/GANT/053/2023/PCBASSEMBLY

Item Name: PCBs Manufacturing and Assembly

1.0 Bidder Eligibility Criteria:

I	**Bidder Eligibility Criteria-I (Public Procurement – Preference to Make in India)**	**Class I / Class II**	**Local Content Percentage**	**Ref. Page No.**
I	Only 'Class-I local suppliers' and 'Class-II local suppliers', as defined under DIPP, MoCI Order No. P-45021/2/2017-PP (BE II) dated 16th September 2020 and other subsequent orders issued therein.			

CHECKLIST

Please ensure that the following compliance sheets are in your technical bid.

Particulars	**Submitted (Yes/No)**
Compliance sheet: 1	
Compliance sheet: 2	
Compliance sheet: 3	
Compliance sheet: SOM	
Compliance sheet: Integrated Mother Board	
Compliance sheet: SOM EVK Mother Board	

The technical details for PCB and assembly are provided below. The BOM for the boards will be providedas Excel sheet upon request. Please email rganti@ee.iitm.ac.in and subashini@5gtbiitm.in

2.0 **Bidder Eligibility Criteria II:**

II	**Bidder Eligibility Criteria-II**	**Complied /Not Complied**	**Ref Page No.**
1	The Firm should have a minimum turnover of 5 crores/year. Evidence should be provided.		
2	The vendor must provide proof of business with other clients (at least 2) in the past year and can provide client references.		
3	The Firm should be in business for a minimum of 5 years. Evidence should be provided.		
4	Please indicate prior High-Speed FPGA and high-power RF boards (of similar complexity of at least 12 layers) that you have fabricated. Vendors without prior experience (of at least two prior boards) of similar complexity will be disqualified. Documentary evidence of the same should be provided.		
5	Explicitly indicate the PCB Fab details for each board and **its technical capabilities**, where each board will be fabricated. References to online material/documentation for verification **should** be provided. The bid might be disqualified if the technical capabilities of the proposed FAB are not clear or do notmeet the technical requirements of the boards. 1. The country of the FAB should explicitly be mentioned. a. If these boards are manufactured in countries that sharea land border with India, the bid will be eligible only if the FAB is registered with the competent authority and the required approvals are obtained as mentioned in the GFR amendments (Rule 144 (xi)) posted on 23rd July 2020. b. These required approvals have to be part of the technical tender for the bid to be valid.		
6	Prior engineering compliance with the FAB (for meeting the technical specifications, as mentioned in the subsequent sections) for manufacturing the required PCB should be provided (for each PCB) in the templates provided in the next sections. 1. The confirmation from the FAB (as email exchange or letters (in English)) should also be provided in the tender. 2. Some important considerations ● Most of the boards require blind vias. ● Impedance control is required		

7	Explicitly indicate the plant details **and its technical capabilities**, where the board will be assembled.		
8	Please indicate the country of the assembly facility. The assembly facility should be in India. ● Where IITM can ship the required components (FPGA's, ICs, Transceivers) ● The assembly plant and testing facility should be in India and should be ready for rework as the case arises without additional cost ● Support for double-sided PCB assembly		
9	Assembly should have the capability of IPC-610 class2 and class 3 standards		
10	The assembly line should be capable of handling 01005 discrete components, 0.4 mm BGA's, 0.4 mm pitch, LGA CC-20-3, and should have the capability of odd angle placement		
11	Assembly Should have the facility for flying probe testers and automated optical lines (inspection)		
12	Assembly should have in house X-ray inspection should be available		

3.0 Technical Compliance:

1) Technical Specifications, quantities for compliance

The following boards are going to be manufactured. All the boards have two stages of manufacturing.

Stage1: PCB fab and assembly for X no of boards. The exact numbers for assembled and bare boards are provided below.

Stage 2: PCB fab and assembly for Y no of boards. The exact numbers for assembled are provided below.

S. No	Board name	Quantity for Stage 1			Quantity for Stage 2	Total Quantity
		Bare Board	Power & Clock Board	Full Assembly	Full Assembly	
1	SOM	1	1	4	14	20
2	Integrated Mother Board	1	0	2	4	7
3	SOM EVK Mother Board	1	0	2	4	7

*There will be minor design changes between Stage 1 and Stage 2.

Compliance Sheet 1

S. No		Complied/ Not Complied
1	There may be design changes in the PCBs (schematics and layout) between Stage 1 and Stage 2. Also a few components (around 5%)might change based on the outcomes of each stage. The Vendor should be able to accommodate these.	
2	Open, Short, and Impedance reports must be submitted before and after Assembly to IIT Madras for validation of the quality of Fabrication and Assembly for 1 st Stage. (Exact Test points Will be shared along with Gerbers)	
3	Complete Test Procedure with detailed Steps will be shared for the 2nd Stage, In addition to Open Short and Impedance testing this includes: 1. Power On test 2. Clock Programming 3. Booting	
4	IIT Madras only will be paying for boards that have passed the tests and been approved and validated by IITM	

Compliance sheet 2

S. No			Complied/Not Complied
1	Turnaround time from the receipt of the PO tillthe fabrication and assembly of the boards for Stage 1	8 Weeks	
2	Turnaround time from the receipt of the go ahead till the fabrication and assembly of the boards for Stage 2	8 weeks	

Terms and conditions.

Compliance sheet 3

S. No		Complied/Not Complied
1	The delivery time cannot be changed	
2	All the boards have been quoted. If some boards are not quoted the vendor will be dis-qualified	
3	The stack up, PCB pre-peg and Core materials of the boards, the via and Trace dimensions and any technical specifications of these boards were **designed after extensivesimulations and will be impossible to change.** **Attached Stack-up has been verified by the following Fabricators:** **1) HiQ** **2) Phase-3** **3) Micro-pack**	

	We encourage the bidders to Fabricate boards from the above Vendors for quick turnaround time. But, bidders are allowed to Fabricate with any other reputed Vendor(as per the tender clauses) as along as the Stack-up and Timeline remains same.	
4	Basic rework might be requested (as required) and the vendor should support this without any additional cost	
5	PCB fabrication: At the end of Stage1, the firm should provide us with a report on the PCBs that were fabricated and assembled and proceed withthe assembly only after technical approval by the IITM team.	
6	In the financial bid, the fabrication cost of each PCB, BOM cost, andAssembly cost are separately and explicitly mentioned.	
7	Will provide the BOM as per the requirements for all the boards. The BOMfor the boards will be provided as excel sheet upon request. Please email rganti@ee.iitm.ac.in and subashini@5gtbiitm.in. Part of the BOM for assembly will be provided by IIT-Madras.	
8	BOM supplied by the Vendor should have warranty and COC certification	

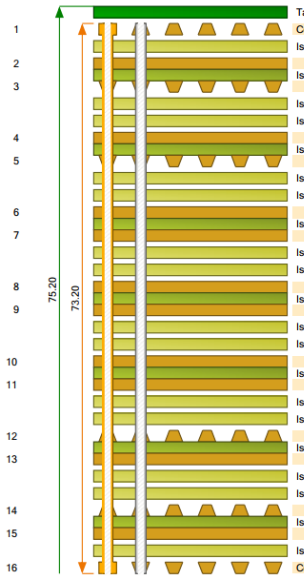
2 BOARD FABRICATION SOM

Compliance Sheet SOM

S. No		Details
1	Country where PCB will bemanufactured	
2	FAB name where PCB will bemanufactured.	
3	FAB technical capability details areprovided (As separate sheets)	
4	Company where PCB will beAssembled in India	

S. No	Description	Specification	Complied/Not Complied
A	**PCB FABRICATION**		
1	No. of layers	16	
2	Via Technology	Through Hole and Blind Via With back drilling option	
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40	
4	Impedance control (Yes/No) Mention tolerance	Yes	
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask	
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: g. Signal Layer Thickness 0.689 mil h. Power (Including ground) layers 0.689 mil and 2.638 mil	
7	Min. finished hole dia (mil)	8 Mil Mech	
8	Min. trace width (mil)	3	
9	Min. spacing (mil)	3	
10	Min. Annular ring (mil)	6	

11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig	
12	PCB Dimension in mm	125 mm X 90 mm +/- 10%	
13	Metal core board	No	
14	Mil Grade	No	
15	Whether Group B Test Report required	No	
16	Solder Mask Colour	Green	
17	Silkscreen Colour	White	
18	RoHS Complaint	Yes	
19	UL Logo Required	Yes	
20	Back Drilling Required	No	
21	RF VIAS	No	
B	**STACKUP REQUIREMENTS**		
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper	
23	Specify Compliance to the Stack up at the bottom		
24	Specify Compliance to the Impedance table at the bottom		
C	**ASSEMBLY**		
25	No of comps per board	1000	
26	No of BGAs per board	10	
27	Maximum pin count	1516, 1 mm BGA	
28	Minimum BGA pitch	1 mm	
29	Total No of points to be soldered (no of Pins)	6000(approx)	
30	PTH pins	300	
31	Both side assembly	Yes	
32	Board Size-	125 mm X 90 mm+/- 10%	
33	Board Thickness	75.196 Mils	
34	No of Layers	16	
35	X-ray verification of all BGA’s, LPA and QFN	Yes. Test results should be provided.	
36	AOI report for the components	Yes, Report needed	
37	Manual Inspection of Q&A for all I. C’s	Yes, Report needed	



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
3			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
5			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
7			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
9			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
11			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
13			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
15			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

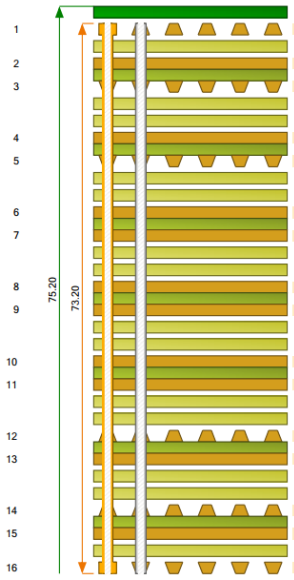
3 BOARD FABRICATION INTEGRATED MOTHER BOARD

Compliance Sheet SOM

S. No		Details
1	Country where PCB will bemanufactured	
2	FAB name where PCB will bemanufactured.	
3	FAB technical capability details areprovided (As separate sheets)	
4	Company where PCB will beAssembled in India	

S. No	Description	Specification	Complied/Not Complied
A	**PCB FABRICATION**		
1	No. of layers	16	
2	Via Technology	Through Hole and Blind Via With back drilling option	
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40	
4	Impedance control (Yes/No) Mention tolerance	Yes	
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask	
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: i. Signal Layer Thickness 0.689 mil j. Power (Including ground) layers 0.689 mil and 2.638 mil	
7	Min. finished hole dia (mil)	8 Mil Mech	
8	Min. trace width (mil)	3	
9	Min. spacing (mil)	3	
10	Min. Annular ring (mil)	6	

11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig	
12	PCB Dimension in mm	125 mm X 90 mm +/- 10%	
13	Metal core board	No	
14	Mil Grade	No	
15	Whether Group B Test Report required	No	
16	Solder Mask Colour	Green	
17	Silkscreen Colour	White	
18	RoHS Complaint	Yes	
19	UL Logo Required	Yes	
20	Blind Vias Buried Vias Back Drilling Required	Yes	
21	RF VIAS	No	
B	**STACKUP REQUIREMENTS**		
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper	
23	Specify Compliance to the Stack up at the bottom		
24	Specify Compliance to the Impedance table at the bottom		
C	**ASSEMBLY**		
25	No of comps per board	500	
26	No of BGAs per board	10	
27	Maximum pin count	540, 1 mm LPGA	
28	Minimum BGA pitch	0.8 mm	
29	Total No of points to be soldered (no of Pins)	6000(approx)	
30	PTH pins	300	
31	Both side assembly	Yes	
32	Board Size-	450 mm X 400 mm+/- 10%	
33	Board Thickness	75.196 Mils	
34	No of Layers	16	
35	X-ray verification of all BGA’s, LPA and QFN	Yes. Test results should be provided.	
36	AOI report for the components	Yes, Report needed	
37	Manual Inspection of Q&A for all I. C’s	Yes, Report needed	



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
3			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
5			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
7			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
9			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
11			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
13			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
15			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

4 BOARD FABRICATION SOM EVK MOTHER BOARD

Compliance Sheet SOM EVK Mother Board

S. No		Details
1	Country where PCB will bemanufactured	
2	FAB name where PCB will bemanufactured.	
3	FAB technical capability details areprovided (As separate sheets)	
4	Company where PCB will beAssembled in India	

S. No	Description	Specification	Complied/Not Complied
A	**PCB FABRICATION**		
1	No. of layers	16	
2	Via Technology	Through Hole and Blind Via With back drilling option	
3	Material (Specify clearly whether High Tg or Normal Tg)	Isola I-TERA MT40	
4	Impedance control (Yes/No) Mention tolerance	Yes	
5	Board thickness (1.6mm/2.4mm/3.2mm/ any other) Mention Tolerance	Entire board must be: 69.496mil thickness over the laminate 73.196mil thickness over the copper 75.196mil thickness over the Solder mask	
6	Copper finish (35 microns/70 microns/ any other)	Copper Thickness: ● Outer Layers: a. Signal Layer Thickness 1.85mil ● Inner Layers: k. Signal Layer Thickness 0.689 mil l. Power (Including ground) layers 0.689 mil and 2.638 mil	
7	Min. finished hole dia (mil)	8 Mil Mech	
8	Min. trace width (mil)	3	
9	Min. spacing (mil)	3	
10	Min. Annular ring (mil)	6	

11	Board finish(Hot Air Levelled/ Electroless Ni-Au / Hard Gold / any other)	Enig	
12	PCB Dimension in mm	170 mm X 170 mm +/- 10%	
13	Metal core board	No	
14	Mil Grade	No	
15	Whether Group B Test Report required	No	
16	Solder Mask Colour	Green	
17	Silkscreen Colour	White	
18	RoHS Complaint	Yes	
19	UL Logo Required	Yes	
20	Back Drilling Required	No	
21	RF VIAS	No	
B	**STACKUP REQUIREMENTS**		
22	Customer required thickness	73.196+/-7.319 mils Measured: Over mask on plated copper	
23	Specify Compliance to the Stack up at the bottom		
24	Specify Compliance to the Impedance table at the bottom		
C	**ASSEMBLY**		
25	No of comps per board	500	
26	No of BGAs per board	10	
27	Maximum pin count	540, 1 mm LPGA	
28	Minimum BGA pitch	0.8 mm	
29	Total No of points to be soldered (no of Pins)	6000(approx)	
30	PTH pins	300	
31	Both side assembly	Yes	
32	Board Size-	125 mm X 90 mm+/- 10%	
33	Board Thickness	75.196 Mils	
34	No of Layers	16	
35	X-ray verification of all BGA’s, LPA and QFN	Yes. Test results should be provided.	
36	AOI report for the components	Yes, Report needed	
37	Manual Inspection of Q&A for all I. C’s	Yes, Report needed	

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
2			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
3			0.689		40.000		7, 8, 9, 10, 11, 12
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
4			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
5			0.689		40.000		13, 14, 15, 16, 17, 18
		Isola I-TERA MT40 PP 1035 RC67	1.890	4.491		3.280	
		Isola I-TERA MT40 PP 1067 RC76	2.601	-		3.080	
6			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
7			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
8			2.638		60.000		
		Isola I-TERA MT40 4 mil core 2/2[2x1035]-VLP2	4.000	4.000		3.280	
9			2.638		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.335	4.669		3.080	
		Isola I-TERA MT40 PP 1067 RC76	2.335	-		3.080	
10			0.689		60.000		
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
11			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
12			0.689		40.000		19, 20, 21, 22, 23, 24
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
13			0.689		60.000		
		Isola I-TERA MT40 PP 1067 RC76	2.601	4.491		3.080	
		Isola I-TERA MT40 PP 1035 RC67	1.890	-		3.280	
14			0.689		40.000		25, 26, 27, 28, 29, 30
		Isola I-TERA MT40 3 mil core H/H[1x1078]-VLP2	3.000	3.000		3.330	
15			0.689		60.000		
		Isola I-TERA MT40 PP 1080 RC70	3.324	3.324		3.210	
16		Copper Foil 12 microns	1.850		100.000		31, 32, 33, 34, 35, 36

75.20

73.20

Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500	

Copper Thickness = 17.245 | Dielectric Thickness = 55.951 | Solder Mask Thickness = 2.000 |Stack Up Thickness = 73.196 | Stack Up Thickness with Soldermask = 75.196

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.400	0.000	0.000	40.100	40.000	10.000
2	1	Coated Microstrip 1B	2	0	6.250	0.000	0.000	50.000	50.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	6.500	4.500	0.000	79.640	80.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	5.600	4.500	0.000	84.850	85.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	4.800	4.500	0.000	90.200	90.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	5.700	0.000	100.120	100.000	10.000
7	3	Edge Coupled Offset Stripline 1B2A	2	4	5.000	5.200	0.000	80.000	80.000	10.000
8	3	Offset Stripline 1B2A	2	4	5.400	0.000	0.000	40.120	40.000	10.000
9	3	Offset Stripline 1B2A	2	4	3.600	0.000	0.000	49.810	50.000	10.000
10	3	Edge Coupled Offset Stripline 1B2A	2	4	3.500	9.000	0.000	99.770	100.000	10.000
11	3	Edge Coupled Offset Stripline 1B2A	2	4	4.500	5.500	0.000	85.040	85.000	10.000
12	3	Edge Coupled Offset Stripline 1B2A	2	4	4.000	5.400	0.000	90.070	90.000	10.000
13	5	Offset Stripline 1B2A	4	6	5.400	0.000	0.000	40.120	40.000	10.000
14	5	Offset Stripline 1B2A	4	6	3.600	0.000	0.000	49.810	50.000	10.000
15	5	Edge Coupled Offset Stripline 1B2A	4	6	3.500	9.000	0.000	99.770	100.000	10.000
16	5	Edge Coupled Offset Stripline 1B2A	4	6	4.500	5.500	0.000	85.040	85.000	10.000
17	5	Edge Coupled Offset Stripline 1B2A	4	6	4.000	5.400	0.000	90.070	90.000	10.000
18	5	Edge Coupled Offset Stripline 1B2A	4	6	5.000	5.200	0.000	80.000	80.000	10.000

Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
19	12	Offset Stripline 1B2A	11	13	5.400	0.000	0.000	40.120	40.000	10.000
20	12	Offset Stripline 1B2A	11	13	3.600	0.000	0.000	49.810	50.000	10.000
21	12	Edge Coupled Offset Stripline 1B2A	11	13	3.500	9.000	0.000	99.770	100.000	10.000
22	12	Edge Coupled Offset Stripline 1B2A	11	13	4.500	5.500	0.000	85.040	85.000	10.000
23	12	Edge Coupled Offset Stripline 1B2A	11	13	4.000	5.400	0.000	90.070	90.000	10.000
24	12	Edge Coupled Offset Stripline 1B2A	11	13	5.000	5.200	0.000	80.000	80.000	10.000
25	14	Edge Coupled Offset Stripline 1B2A	13	15	5.000	5.200	0.000	80.000	80.000	10.000
26	14	Offset Stripline 1B2A	13	15	5.400	0.000	0.000	40.120	40.000	10.000
27	14	Offset Stripline 1B2A	13	15	3.600	0.000	0.000	49.810	50.000	10.000
28	14	Edge Coupled Offset Stripline 1B2A	13	15	3.500	9.000	0.000	99.770	100.000	10.000
29	14	Edge Coupled Offset Stripline 1B2A	13	15	4.500	5.500	0.000	85.040	85.000	10.000
30	14	Edge Coupled Offset Stripline 1B2A	13	15	4.000	5.400	0.000	90.070	90.000	10.000
31	16	Coated Microstrip 1B	15	0	9.400	0.000	0.000	40.100	40.000	10.000
32	16	Coated Microstrip 1B	15	0	6.250	0.000	0.000	50.000	50.000	10.000
33	16	Edge Coupled Coated Microstrip 1B	15	0	6.500	4.500	0.000	79.640	80.000	10.000
34	16	Edge Coupled Coated Microstrip 1B	15	0	5.600	4.500	0.000	84.850	85.000	10.000
35	16	Edge Coupled Coated Microstrip 1B	15	0	4.800	4.500	0.000	90.200	90.000	10.000
36	16	Edge Coupled Coated Microstrip 1B	15	0	4.200	5.700	0.000	100.120	100.000	10.000

TWO STAGE PAYMENT

Stage 1:40% Payment will be done once the stage 1 is completed and is delivered.
Stage 2:60% Payment will be done once the stage 2 is completed and is delivered.

SIGNATURE OF BIDDER ALONG WITH SEAL OF THE COMPANY WITH DATE

ANNEXURE - C

FINANCIAL BID (PROFORMA) - BILL OF QUANTITIES (BOQ)

Item Name: PCBs Manufacturing and Assembly
Tender No: EE/GANT/053/2023/PCBASSEMBLY

It. No	Description of work	Quantity	Units	Basic unit cost in INR	GST in Percentage	Total Amount with taxes in INR
1	SOM BOM Cost	19	Nos.			
2	Integrated Mother Board BOM Cost	6	Nos.			
3	SOM EVK Mother Board BOM Cost	6	Nos.			
4	SOM Fabrication Cost	20	Nos.			
5	Integrated Mother Board Fabrication Cost	7	Nos.			
6	SOM EVK Mother Board Fabrication Cost	7	Nos.			
7	SOM Assembly Cost	19	Nos.			
8	Integrated Mother Board Assembly Cost	6	Nos.			
9	SOM EVK Mother Board Assembly Cost	6	Nos.			
	Grand Total					

Total Amount Rupees in words _____

ANNEXURE – D

FORMAT FOR AFFIDAVIT OF SELF-CERTIFICATION UNDER PREFERENCE TO MAKE IN INDIA – PER ITEM

Tender Reference Number:

Name of the item / Service:

Date: _____
I/We_____S/o, D/o, W/o, _____
Resident of
_____

Hereby solemnly affirm and declare as under:

That I will agree to abide by the terms and conditions of the Public Procurement (Preference to Make in India) Policy vide GoI Order no. P-45021/2/2017-PP (B.E.-II) dated 15.06.2017 (subsequently revised vide orders dated 28.05.2018, 29.05.2019and 04.06.2020) MOCI order No. 45021/2/2017-PP (BE II) Dt.16th September 2020 & P- 45021/102/2019-BE-II-Part (1) (E-50310) Dt.4th March 2021 and any subsequent modifications/Amendments, if any and

That the local content for all inputs which constitute the said item/service/work has been verified by me and I am responsible for the correctness of the claims made therein.

Tick (✓) and Fill the Appropriate Category	
☐	I/We_____[name of the supplier] hereby confirm in respect of quoted items thatLocal Content is equal to or more than 50% and come under **"Class-I Local Supplier"** category.
☐	I/We_____[name of the supplier] hereby confirm in respect of quoted items that Local Content is equal to 20% but less than 50% and come under **"Class-II Local Supplier"** category.

- The details of the location (s) at which the local value addition is made and the proportionate value of local content in percentage

Address _____ _____ __ Percentage of Local content: _____%
_____

For and on behalf of.....(Name of firm/entity)

Authorized signatory (To be duly authorized by the Board of Directors)
<Insert Name, Designation and Contact No.>

[Note: In case of procurement for a value in excess of Rs. 10 Crores, the bidders shall provide this certificate fromstatutory auditor or cost auditor of the company (in the case of companies) or from a practicing cost accountant or practicing chartered accountant (in respect of suppliers other than companies) giving the percentage of local content.]

This letter should be on the letterhead of the quoting firm and should be signed by a competent authority. Non-submission of this will lead to Disqualification of bids.

ANNEXURE – E

(To be given on the letter head of the bidder)

No._____ Dated: _____

CERTIFICATE

(Bidders from India)

I have read the clause regarding restrictions on procurement from a bidder of a country which shares a land border with India and hereby certify that I am not from such a country.

OR *(whichever is applicable)*

(Bidders from Country which shares a land border with India)

I have read the clause regarding restrictions on procurement from a bidder of a country which shares a land border with India and hereby certify that I from _____ (Name of Country) and has been registered with the Competent Authority. I also certify that I fulfil all the requirements in this regard and is eligible to be considered. *(Copy/ evidence of valid registration by the Competent Authority is to be attached)*

Place:
Date:

Signature of the Tenderer
Name & Address of the Tenderer with

Office Stamp

ANNEXURE - F

OEM CERTIFICATION FORM
(In Original Letter Head of OEM)

Tender No: ..... Dated: .....

We are Original Equipment Manufacturers (OEM) of..... (Name of the company)

Ms..... (Name of the vendor) is one of our

Distributors/Dealers/Resellers/Partners (tick one) for the

……. and is participating in the above-

mentioned tender by offering our product model.....(Name of the product with

model number).

…….. is authorized to bid, sell and provide service support warranty for our product
as mentioned above.

Name and Signature of the authorized
signatory of OEM along with
seal of the company with Date

ANNEXURE - G

TENDER CHECKLIST – Mandatory to be filled and sent (inside the Main Bid Cover) along with Bidding Document.

(1) I have registered as a Vendor with IC&SR. (Proof to be enclosed) ☐

(2) Technical bid cover and Financial Bid cover to be submitted separated. ☐

(3) Completed and **Signed Form of Tender**. The Form of Tender document shall be signed by a person legally authorized. ☐

(4) Completed Technical Compliance Statement ☐

(5) Certification of Class I / Class II (**As a part of technical bid) per item / service / work as per (Annexure – D)** ☐

(6) EMD (Ref. tender document pg.no. 6, Point no.9) ☐

(7) Land Border **(Annexure – E)** ☐

(8) Authorized agent certificate from OEM is mandatory if Indian agent/Indian office of OEM is participating in this tender on behalf of OEM. ☐

The bid will be valid only if all the above documents are provided. Bidders are asked to supply and tick off the required information. Failure to provide any of the stated documents may result in the bid being considered as non-compliant and rejected.

Signature of the Bidder

ANNEXURE - H

FORM - A
NON-BLACKLISTING DECLARATION

Date: XXXX

To,
The Indian Institute of Technology Madras,
Sardar Patel road,
Guindy, Chennai - 600036

Subject: Non-Blacklisting declaration in connection with tender RFF No: XXXXXX for procurement of "XXXXXXXXXXXXXXXXXXXXXXXXXXXX"

Dear Sir,

This is to notify you that our Firm/Company/Organization <*provide Name of the Firm/Company/Organization*> intends to submit a proposal in response to the invitation for procurement of "XXXXXXXXXXXXXXXXXXXXXXXXXXXX" In accordance with the above we declare that:

a. We are not involved in any major litigation that may have an impact of affecting or compromising the delivery of services as required under this assignment.

b. We are not blacklisted by any Central/ State Government/ agency of Central/ State Government of India or any other country in the world/ Public Sector Undertaking/ any Regulatory Authorities in India or any other country in the world for any kind of fraudulent activities in last XX years.

Sincerely,

[BIDDERS NAME]
Name
Title Signature

CENTRE FOR INDUSTRIAL CONSULTANCY & SPONSORED RESEARCH (IC&SR)
INDIAN INSTITUTE OF TECHNOLOGY MADRAS
CHENNAI 600 036

ELECTRONIC CLEARING SERVICE (Credit Clearing)/ REAL TIME GROSS SETTLEMENT (RTGS) FACILITY FOR RECEIVING PAYMENTS

A. Details of Account Holder

Name of the Institution	Indian Institute of Technology - Madras
Complete Contact Address	Industrial Consultancy and Sponsored Research Indian Institute of Technology-Madras, IIT- Madras Campus Post Office, Sardar Patel Road, Guindy, CHENNAI - 600 036
Telephone No./ Fax No.	Tel - 044-2257 8356
E- mail ID of the FO/AO/REG/DIR	dricsr@iitm.ac.in

B. Bank Account Details:

Institution Account Name (As per Bank Record)	The Registrar, Indian Institute of Technology - Madras
Account No.	2722101003872
Account Print Name	IIT F A/C , The Registrar IIT Madras
IFSC CODE	CNRB0002722
Bank Name (in full)	Canara Bank
Branch Name	IIT-Madras Branch
Complete Branch Address	Canara Bank, IIT-Madras Branch, IIT- Madras Campus Post Office, Sardar Patel Road, Guindy, CHENNAI - 600 036
MICR No.	600015085
Account Type	Savings Account

Certified that the Institute's account is in an RTGS enabled branch.
I hereby declare that the particulars given above are correct and complete.

Date: 19/10/2020

Signature of the Competent Authority
of the Institution with seal.